IRIS Crimson Installation and Configuration Guide

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Contributors

Written by Pablo Rozal
Edited by Loraine McCormick
Production by Lorrie Williams
Illustrations by Dan Young
Engineering contributions by David Alexander, John Burger, Keith Matasci, Dana Crom, Kevin Gorey, Paul Hugo, Judy Bergwerk, Tom Mitchell, Dilip Patel, Eugene Yu, Ermalinda Horne, David Laird

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Document Number 108-7034-020

Silicon Graphics, Inc.
Mountain View, California

Contents

Figures

Tables

Chapter 1

General Information

This guide provides a product description, installation, and configuration information for the IRIS® Crimson™ system. See Figure 1-1. This information is written for system support engineers (SSEs), field engineers, or other Silicon Graphics® certified technical personnel.

1.1 Product Description

Major features of the Crimson system include:

- IP17 (R4000 50 MHz) CPU
- Entry, Elan, PowerVision™, or, RealityEngine™ graphics capability
- Single Tower chassis style (with 4 VME slots)

The Crimson also comes standard with the IO3B (POWER Channel™) board that is specially designed to work with the IP17 CPU.

Note: The IP17 (R4000) CPU board comes only in a single processor configuration. You cannot add other CPU boards to an IP17 system.

Other distinguishing features of Crimson include:

- superpipelined R4000SC (secondary cache) processor clocked externally at 50 MHz (100 MHz internally), with 1 MB second-level cache.
- high performance I/O subsystem that includes a VME bus, Ethernet®, and two small computer systems interface (SCSI) channels with disk striping support.
- from 16 MB to 256 MB of RAM, with internal disk capacity of up to 3.6 GB. In addition, the IRIS Crimson can support up to 100 GB of storage, using additional enclosures such as the POWER Store™ rack.

  Note: You can install main memory on the IP17 CPU board only. You cannot install an MC2 memory board into a Crimson system.
- complete networking support, including fiber distributed data interface (FDDI) and high performance parallel interface (HPPI).
- upwardly binary compatible with all existing Silicon Graphics IRIS-4D™ systems.
- front loading devices (FLDs): tape and disk drives.

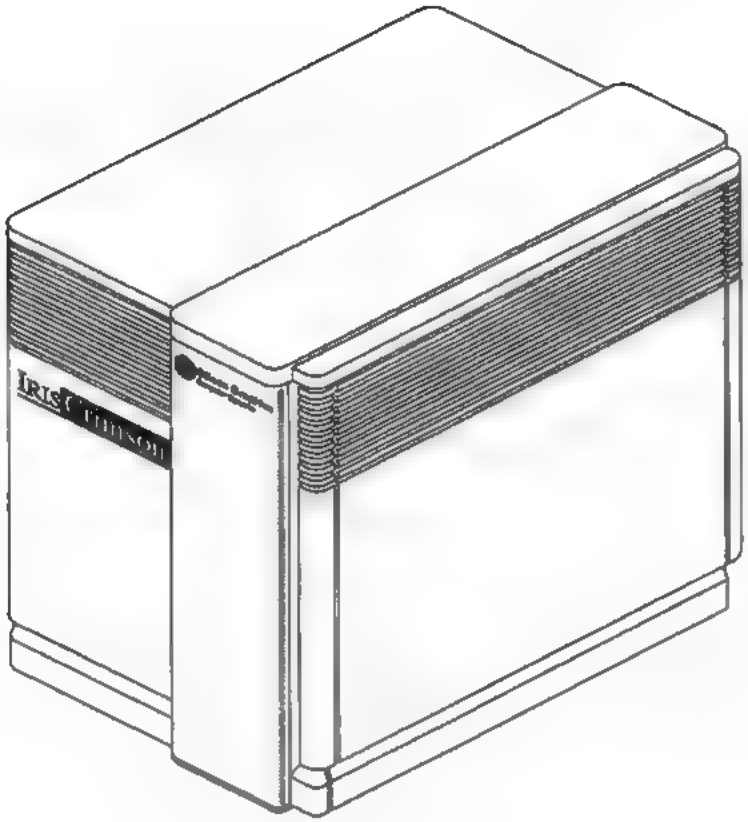


Figure 1-1 IRIS Crimson System (Front View)

- serial I/O board with three DIN and four D-sub connectors.
- status LED and power-on DIP switches located behind status panel.
- thermostatic fan controller for quieter operation.
- improved backplane design; if VME boards are installed from left to right with no gaps, the VME slots no longer require jumper block removal and replacement.

1.2 Product Line Structure

The Crimson provides a mid-scale product alternative between the POWER Series™ and Personal IRIS™ systems in the Silicon Graphics product line. See Figure 1-2.

1.3 Configurations

The Crimson has two basic configurations:

- server
- graphics

The Crimson provides many graphic configurations. Major graphics configurations include the Entry and Elan graphics. Other major configurations are the PowerVision (VGX/VGXT) and RealityEngine graphics. These configurations are detailed in Chapter 2, "Configurations and Components."

1.4 Other Crimson Product Names

Table 1-1 lists alternate names that may be used within Silicon Graphics to describe the same item.

Names Used in This Guide	Silicon Graphic Aliases
Entry	Starter* or Base Level Graphics (BLG) system
XS, XS24, Elan graphic boards	Express* graphic boards
MG1/graphics board	GRINCH board
Crimson bus	MP bus

*Starter and Express are IRIS Indigo™ equivalents for the IRIS Crimson.

Table 1-1 Alternate Crimson Product Names

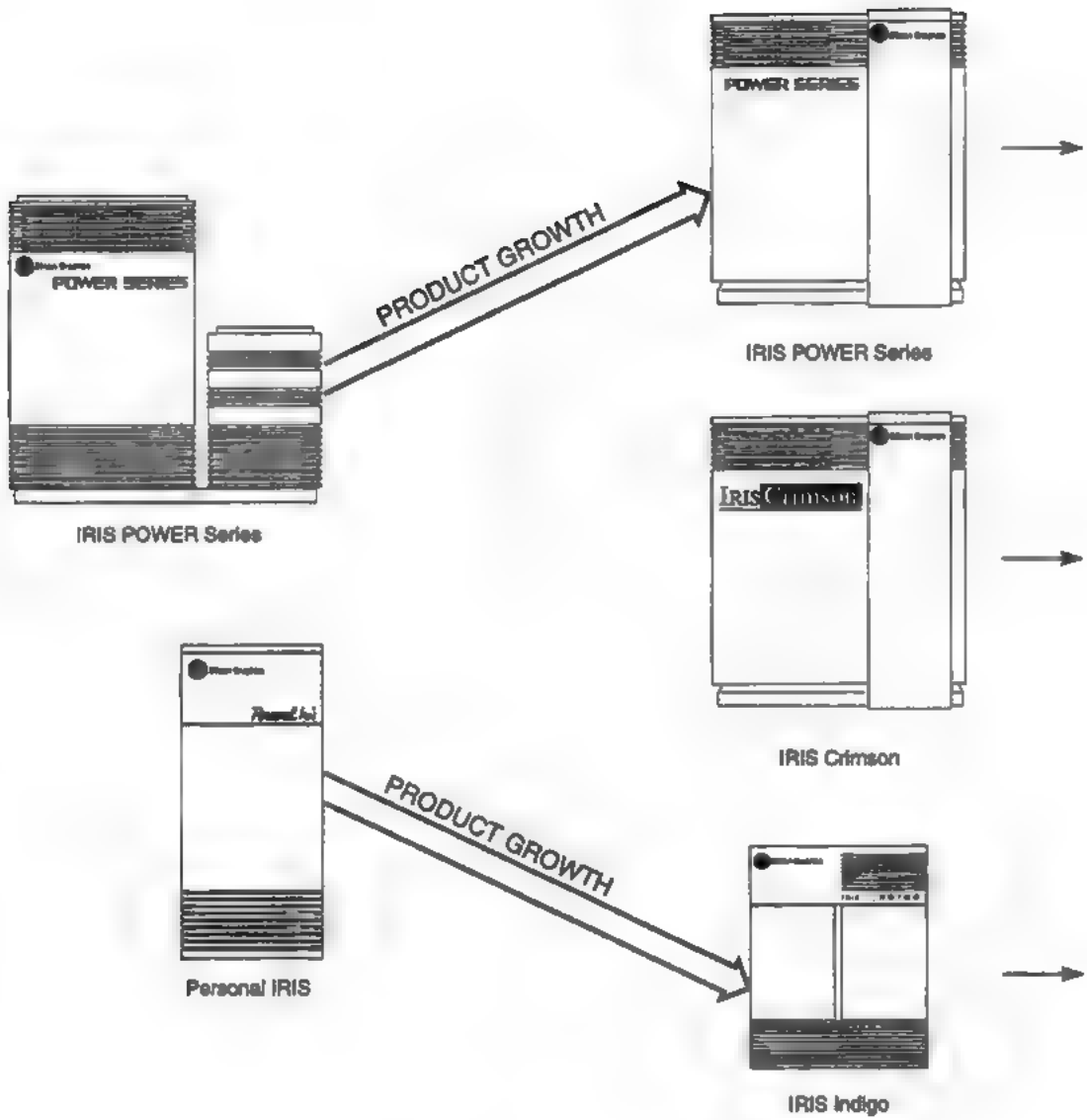


Figure 1-2 Silicon Graphics Product Structure (Simplified)

1.5 Functional Description

The following section provides a functional description of the Crimson system. Figure 1-3 shows a system block diagram.

1.5.1 System Architecture

The IRIS Crimson uses the Crimson Bus, a version of the MPLink bus modified for single processor operations and a sustained throughput of 64 MB per second. The CPU communicates with the graphics and input/output (I/O) subsystems through this bus.

Note: The Crimson and CPU buses are clocked independently to run at maximum performance.

The CPU board uses several custom application-specific integrated circuits (ASICs) designed by Silicon Graphics to maximize throughput as follows:

- RCB ASIC
- RMI ASIC
- CBMI ASIC
- Memory and DCC ASIC

These chips manage memory and processor interrupts, handle I/O, control the bus, fill pixels and draw lines, control graphics output, and access color tables, often without CPU intervention.

RCB ASIC

The R4000SC to Crimson Bus interface (RCB) ASIC allows the R4000SC access to local I/O and the Crimson Bus for programmed I/O (PIO), direct memory access (DMA) and 3-way transfers through uncached load and store operations.

The RCB connects to a 16 MHz multiplexed address and data bus. The pins go to two sets of external addresses and data registers, one for the local I/O bus and the other for the Crimson bus interface.

The local I/O bus provides address, data, and control signals to interface with the EPROMs, EEPROM, DUARTs, timers, status LED, and the sync bus chip.

The Crimson bus master interface includes request logic for gaining bus ownership for performing PIO, DMA, and 3-way transfer operations. The Crimson bus arbiter, which is located on the IO3B board, has been enhanced so that the CPU Crimson bus request has highest priority by default.

The RCB also connects to the R4000SC through the 64-bit address and data bus. It monitors the 50 MHz bidirectional buses when the R4000SC issues a processor request and drives them when issuing an external request.

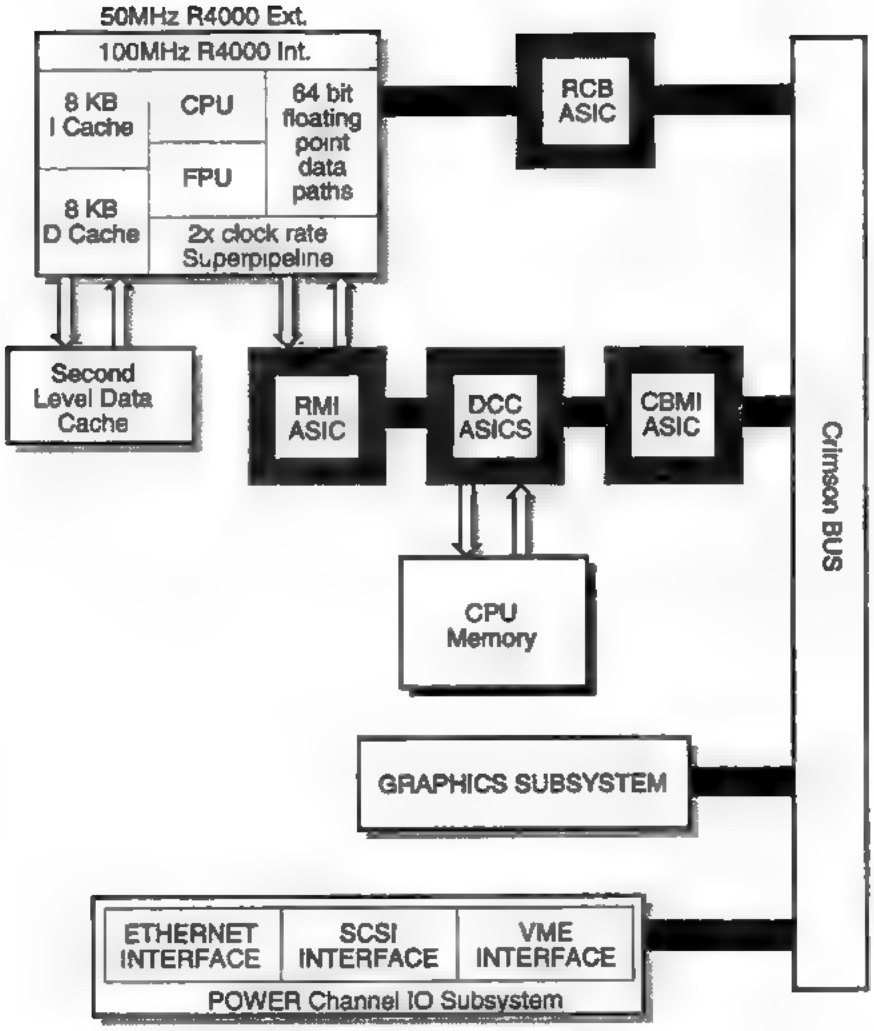


Figure 1-3 IRIS Crimson System Block Diagram

RMI Interface ASIC

The R4000SC to memory interface (RMI) ASIC provides the R4000SC access to main memory through block transfers in the event of a secondary cache miss. The RMI is one of two requesters that contend for access to main memory.

The RMI contains arbitration logic that coordinates access to memory. As stated earlier, the CPU has default accessibility. The other memory requester, the Crimson Bus, is allowed access only when the RMI has completed its current block transfer, if in progress. The RMI is also responsible for generating refresh commands to the DRAM memory system.

CBMI ASIC

The Crimson bus-to-memory interface (CBMI) ASIC provides Crimson bus DMA masters access to the on-board memory during DMA transfers. The CBMI provides primarily a 64-bit data path between the Crimson bus and on-board memory.

The CBMI connects to the external bus drives and provides a Crimson bus slave interface similar to the current MC2 (external) memory board. Control logic and state machines contained in the CBMI provide the timing and sequencing for DMA read and DMA write transfers.

Memory and DCC ASIC

The dynamic RAM Control (DCC) ASICs control access to the on-board DRAM memory. The memory can operate at either 50 MHz (for the R4000) or 16 MHz (for the Crimson bus).

The on-board memory is expandable from 64 to 256 MBs using 8 MB SIMMs or 16 to 64 MBs with 2 MB SIMMs.

Note: For complete memory installation information on the IP17 CPU board, see Chapter 5, "Installation."

1.5.2 Entry Graphics Subsystem

The Crimson/Entry system or base level graphics (BLG) configuration is designed primarily for computation and secondarily for graphics display. The Entry graphics contains the following subsystems. See also Figure 1-4.

- Raster Engine (REX) ASIC converts geometric data processed by the CPU into pixel and line data and then writes this information into the frame buffer.
- The frame buffer (VRAM) contains the pixel color and overlay data for the 1024 x 768 display.
- The video controller (VC1) ASIC, color lookup table (LUT1) ASIC, and 24-bit digital-to-analog converter (DAC) generate the RGB video signals sent to the monitor.

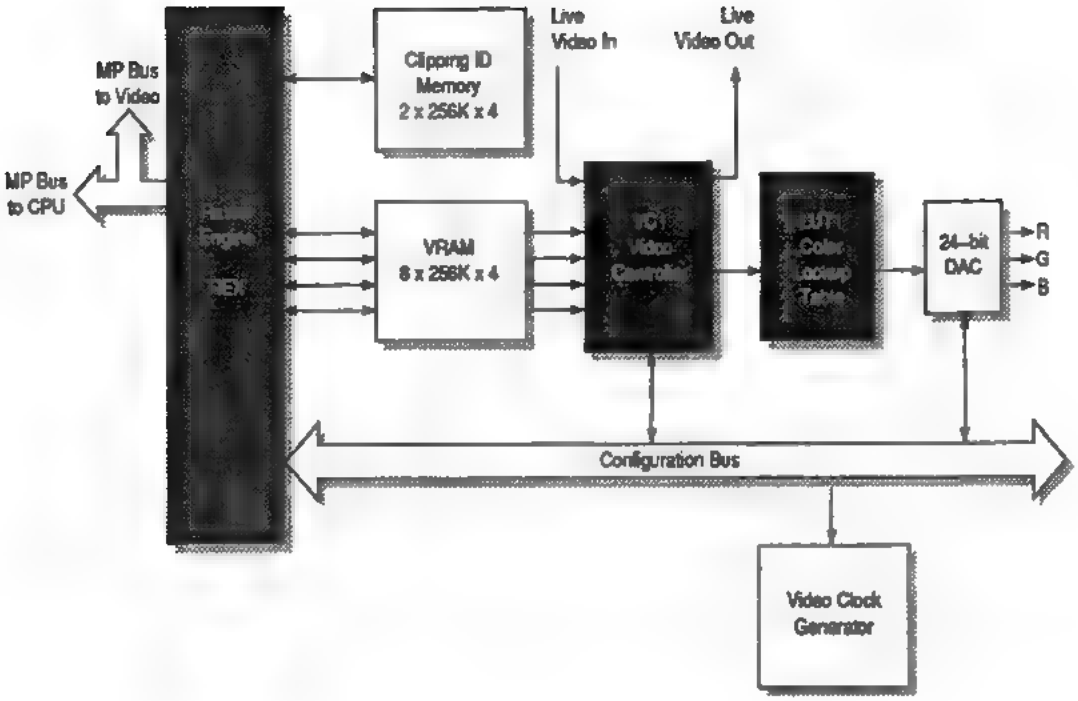


Figure 1-4 Entry Graphics Block Diagram

Note: Much of the Entry graphics functionality is built into software and does not require dedicated video RAM.

Entry graphics uses an innovative approach to provide z-buffering (depth information used for rendering). Instead of using dedicated RAM for the z-buffer, the CPU board calculates and stores z-buffer values in dynamically allocated main memory, creating a virtual z-buffer of 32-bit depth. This not only keeps costs low by using general RAM instead of dedicated RAM, but also surpasses the standard IRIS z-buffer depth of 24 bits and increases the resolution for determining depth.

The main bus on the Crimson Entry Graphics board, the Configuration bus, provides a communication path between the elements of the graphics subsystem. The Entry graphics board is connected to the GIO32 bus through the REX ASIC.

Graphics Display Subsystem

The graphics display subsystem generates the graphics signal sent to the IRIS Crimson color monitor. This subsystem has four major parts; two are implemented as custom ASICs:

- the video controller (VC1) ASIC
- the color lookup table (LUT1) ASIC
- a graphics clock generator
- a 24-bit DAC that produces RBG output to the monitor

The VC1 ASIC takes pixel and overlay values from the VRAM and commands from REX and produces video timing signals and 10-bit indices for the color lookup table (LUT1). It also generates the cursor and maintains the display IDs. The VC1 is a high-density ASIC designed by Silicon Graphics.

1.5.3 Elan Graphics

In addition to Entry graphics features, the Elan graphics configurations offer Geometry Engine™ processing, solids modeling capability, and z-buffering hardware. The Elan graphics also supports 1280 x 1024 screen resolution. Elan graphics are available in three configurations:

- IRIS Crimson/XS with 8-bit dithered color and optional 24-bit z-buffer
- IRIS Crimson/XS24 with 24-bit color and optional 24-bit z-buffer
- IRIS Crimson/Elan with 24-bit color and standard 24-bit z-buffer

Features

Elan graphics provide the following features:

- 24-bit color (XS/24 and Elan configurations only; optional on the XS)
- 4 stencil bitplanes (Elan configuration only; optional on XZ and XS/24)
- 4 overlay and 4 window ID planes
- 32 different simultaneous window modes
- Screen refresh rate at 60 Hz and 72 Hz
- Support for live video in and out (NTSC and PAL video timings)
- Genlock capability
- Stereo viewer control

Elan Graphics Architecture

The Elan graphics system is connected to the CPU subsystem through the 32-bit GIO32 bus and the Crimson graphics interface channel. Drawing commands in conjunction with world coordinate geometric data are passed across the GIO32 bus and written into the graphics input FIFO. The graphics FIFO buffers differences in computation latencies between the CPU application program and the graphics engines. The FIFO is implemented as a sub-block inside the HQ2 chip gate array.

The Crimson Elan graphics architecture performs transformations and other graphics operations to calculate specific pixel values for each of the 1.3 million pixels on the 1280 x 1024 high resolution display. Visual data from the RISC host is processed through five pipelined graphics subsystems before being displayed on the screen. See Figure 1-5.

The Elan graphics circuitry has five graphics subsystems:

command engine (CE)
: monitors the output of the graphics FIFO and passes the data to the Geometry Engine. The CE also converts all incoming data words to a uniform floating point format, regardless of the input data representation. The Command Engine is implemented as a micro programmed processor running inside the HQ2 gate array.

GE7 Geometry Engine (GE)
: a custom floating point data path designed by Silicon Graphics is at the heart of the geometry subsystem. Four GEs execute together as an SIMD machine under the control of a centralized sequencer in the HQ2.

raster subsystem
: reduces a vector or triangle description to individual pixels that are written into the frame buffer. The RE3 is a major component in this subsystem. The RE3 accepts initial pixel values and parameter slopes from the geometry subsystem, and it provides information to iterate either a vector or a triangle.

frame buffer
: receives the output pixel value from the RE3. This 5-way frame buffer stores a total of 56 bits (including the z-buffer) for every pixel on a 1280 x 1024 screen.

display subsystem
: receives pixel information from the frame buffer, routes it through the appropriate display mode, and sends it to the digital-to-analog converters (DACs) for display.

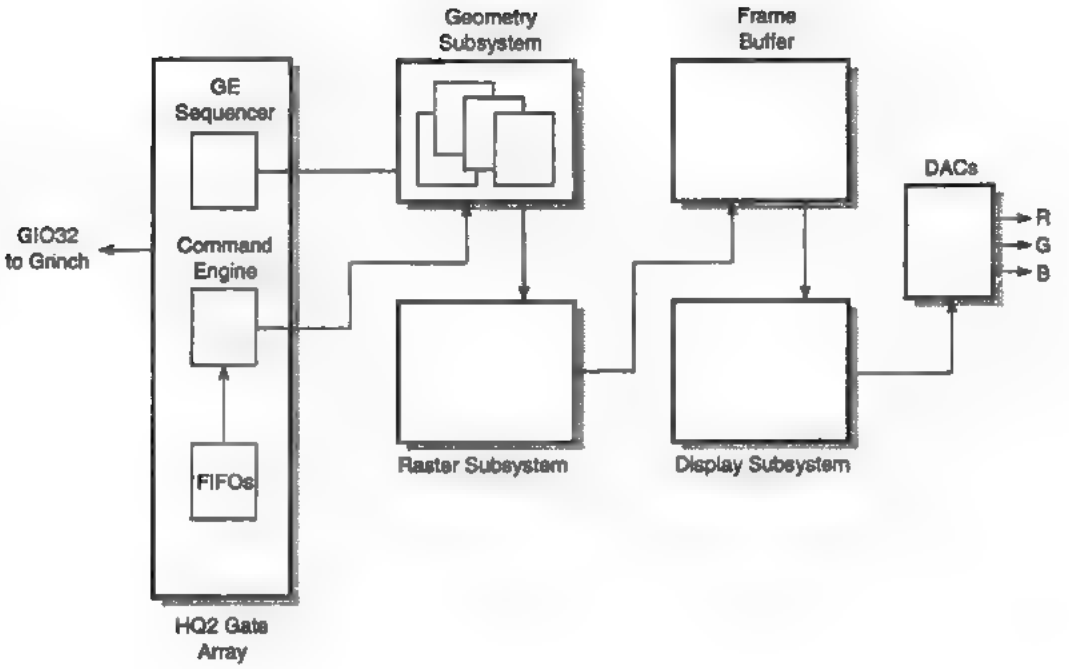


Figure 1-5 Elan Graphics Block Diagram

Video Timing Control

The VCI gate array handles the video timing control, window display mode control, and cursor control. Video timing determines the relationship between active pixels, blanking periods, and sync times. These relationships vary from monitor to monitor. The Crimson Elan supports the following monitor types:

- 72 Hz (1280 x 1024)
- 60 Hz (1280 x 1024)
- 30 Hz (1280 x 1024)
- 72 Hz (1024 x 768)
- 60 Hz (1024 x 768)

- 30 Hz (1024 x 768)
- NTSC (unencoded)
- PAL (unencoded)
- 120 Hz (1280 x1024 stereo)
- 120 Hz (1024 x 768 stereo)

1.5.4 MG1 (GRINCH) Board

The MG1 or GRaphics INterface CHannel (GRINCH) board resides in a 9U, extender board assembly next to either the Entry or Elan board. See Figure 1-6. The MG1/graphics board converts the graphics input/output (GIO) bus signals used by the graphics subsystems into Crimson bus signals.

The graphics board that is installed next to the MG1/graphics board has a built-in 13W3 cable connector that mounts on the I/O panel.

The MG1/graphics board consists of the following major logic blocks (see Figure 1-7):

MP (or Crimson) bus interface and control logic
: a modified version of the MP Link bus. The interface consists of drivers and receivers. The control logic controls data movement to and from the bus.

MG1 flash EPROM
: a 1-Mbit (128k x 8 bit) wide device that can be read or *written* to by software. This allows upgrades to be added to the Crimson graphics board without physically changing the PROM.

  The EPROM contains both Starter and Elan graphics code. It also provides a common CPU interface for detecting and booting the graphics system.

command mapping RAM
: used only in 3-way transfers. The mapper takes a combinational address from the MP bus and looks up the corresponding 24-bit GIO address.

data and address FIFO buffers
: provide an interrupt to the MP bus when it is half full to balance the fill and empty rates.

GIO control and interface logic
: consists of drivers and receivers. The control logic controls data movement to and from the bus.

Note: Special write registers enable data to be written to the GIO bus that bypass the FIFOs for priority PIO word writes and diagnostics. See Figure 1-7.

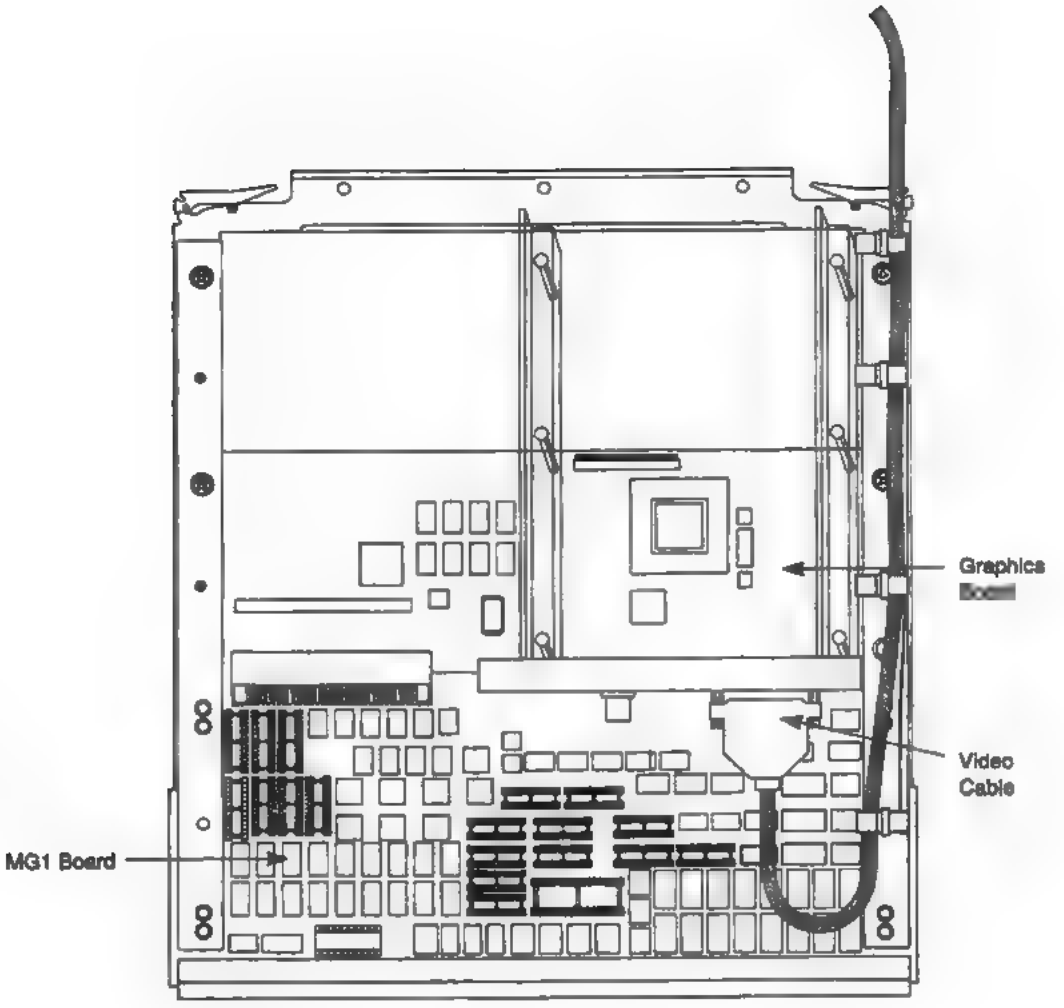


Figure 1-6 The Crimson MG1/Graphics Board

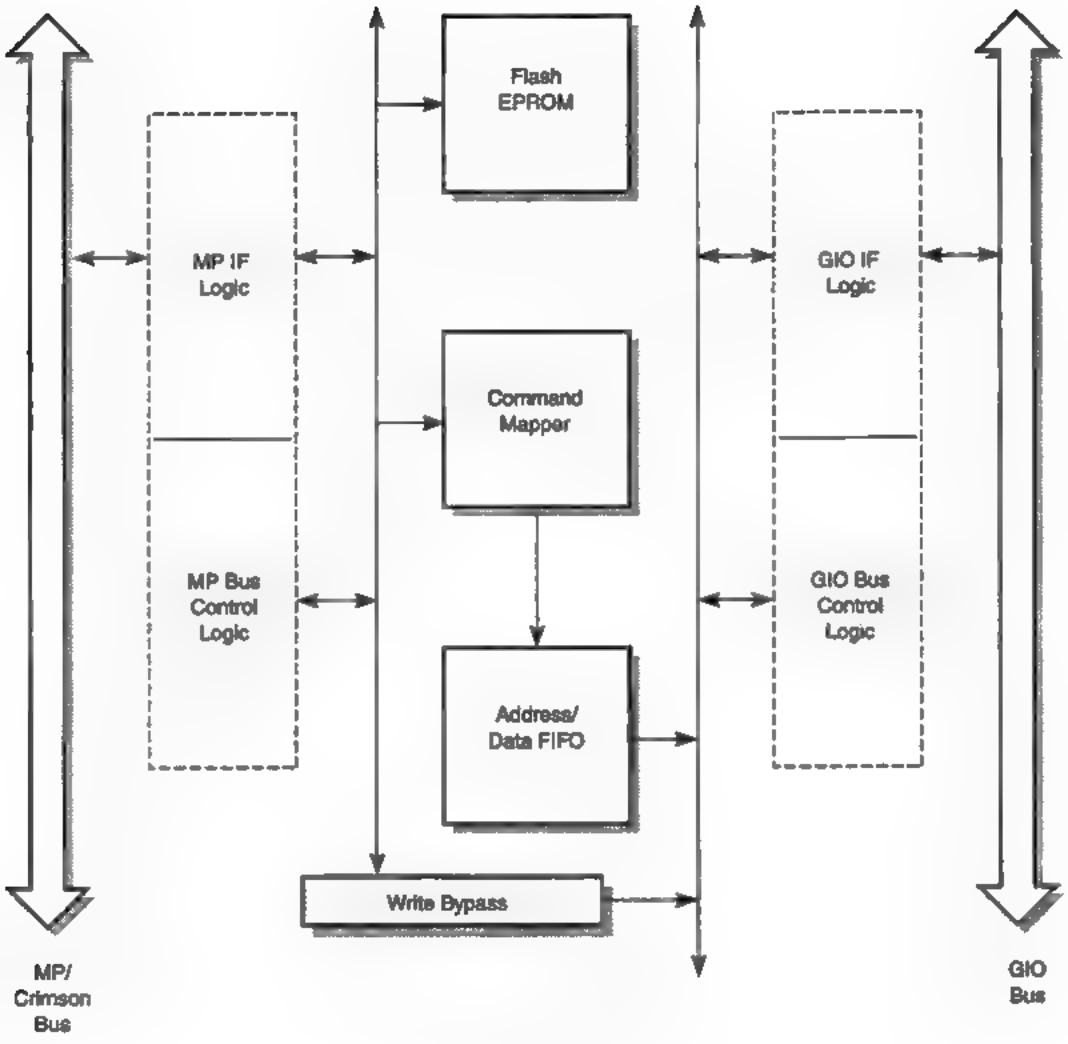


Figure 1-7 The Crimson MG1 Board Block Diagram

Chapter 2

Configurations and Components

This chapter describes the available system versions and the components for each IRIS Crimson system configuration.

2.1 Server System

The following describes the Crimson Server configuration (W6-4DCRIMS) and associated components list.

2.1.1 Configuration

The server system comes standard with an IP17 (50 MHz) CPU board and POWER Channel IO3B board. This configuration contains no graphics board.

Note: There is also a server configuration that contains 64 MB of main memory. The marketing code for this configuration is W6-4DCR64S.

2.1.2 Components List

Table 2-1 lists the various components of the Crimson Server system.

Item No.	Part Number	Description
1	013-0386-xxx	TOP ASSY,DIEHARD MP
2	021-0054-xxx	DWG,SKINNING AND LABELING,DIEHARD
3	040-0220-xxx	WHEEL CHOCK
4	024-0541-xxx	LABEL,SET,SYSTEM,SGI
5	030-0222-xxx	PCB ASSY,IO3B,TESTED
6	0006 018-0172-xxx	CABLE ASSY,SCSI
7	026-0686-xxx	KIT,DIEHARD SHIPPING CONTAINER
8	026-0691-xxx	SKIN KIT,CRIMSON
9	030-0212-xxx	PCB ASSY,IP17,TESTED
10	013-0450-xxx	DRIVE DOOR ASSY,CLOVER GRAY
11	050-0006-xxx	TOPHAT,CLOVER GRAY
12	007-0610-xxx	MNL,IRIS-4D SYS TUNING CONFIG GUID
13	024-0559-xxx	LABEL,TOP HAT,CRIMSON,SERVER
14	9090817	CONN TERM 50P2R M SHLDSE 330/220RES
15	007-1540-xxx	MNL,CRIMSON OWNER'S GUIDE
16	9980027	SCREW,8-32X3/8L,TAMPER PROOF
17	9980028	COLLAR,STEEL,(TAMPER PROOF SCREW)
18	7280075	WASHER,FL,.173 IDX.625 ODX.03THK,ST
19	7420013	ADHESIVE,THREADLOCKING,10ML BTL
20	9750002	RETAINER,PCB,12.30" LONG
21	9770001	LATCH, PCB RETAINER
22	024-0483-xxx	PLATE, CONN MOUNTING, 19" RACK
23	7270119	SCREW,4-40X1/4,HEX WSHR HD STL ZNC
24	108-7034-xxx	MNL,CRIMSON CONF & INST GUIDE
25	026-0761-xxx	KIT,DIEHARD SHIPPING LABELS
26	013-0386-xxx	TOP ASSY,DIEHARD MP

Table 2-1 Crimson Server (W6-4DCRIMS) Parts List

2.2 Graphics System Configurations

The Crimson system comes in eight graphics configurations as follows (marketing codes are in parentheses):

- Crimson/Entry (W6-4DCRIMBLG)
- Crimson/XS (W6-4DCRIMXS)
- Crimson/XS24 (W6-4DCRIMXS24)
- Crimson/Elan (W6-4DCRIMEG)
- Crimson/VGX (W6-4DCRIMVGX)
- Crimson/VGXT (W6-4DCRIMVGXT)
- Crimson/RealityEngine with 16 MB (W6-4DCRIMRE)
- Crimson/RealityEngine with 64 MB (W6-4DCR64RE)

Note: All graphics configurations come standard with an IP17 CPU board and POWER Channel IO3B board. Each of these configurations also comes in a 64 MB version. The marketing codes for these versions use this format: W6-4DCR64BLG (Crimson/Entry), W6-4DCR64XS (Crimson/XS), etc.

2.2.1 Crimson/Entry

The Crimson/Entry or base-level graphics (BLG) system contains an 8-bitplane subsystem and includes software z-buffering and hardware-assisted dithering to produce 24-bit color. The screen resolution is 1024 x 768. Figure 2-1 illustrates the Entry graphics board.

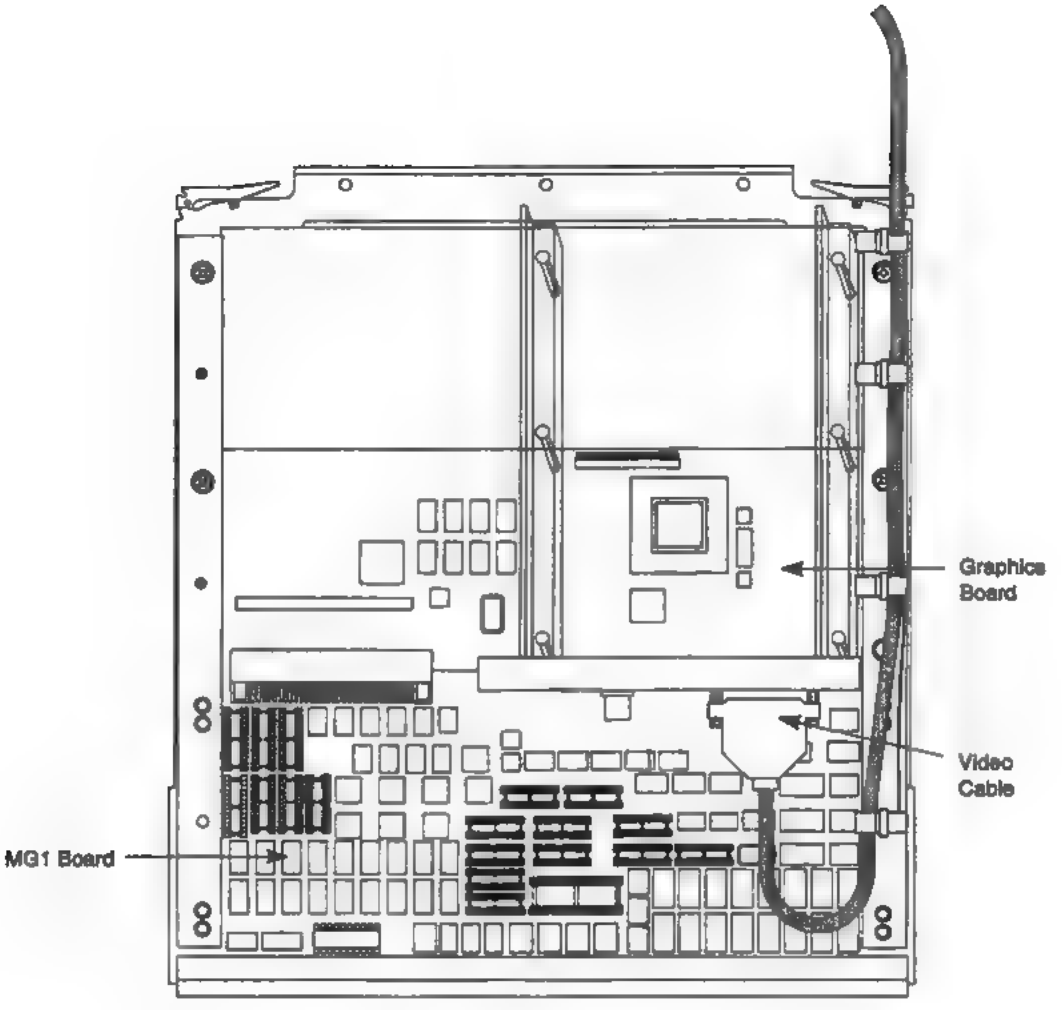


Figure 2-1 Entry Graphics Board

2.2.2 Crimson/XS

The XS configuration includes all Entry features, plus a larger screen resolution (1280 x 1024), optional hardware z-buffering, and one Geometry Engine processor to increase polygon performance. Figure 2-2 illustrates the XS graphics board.

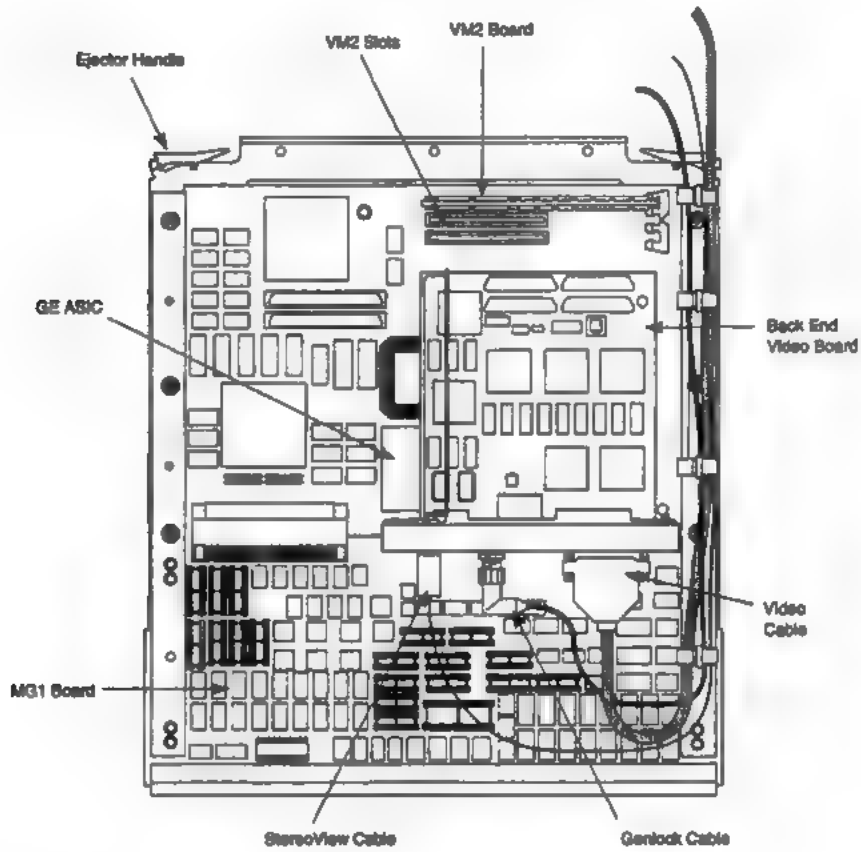


Figure 2-2 XS Graphics Board

2.2.3 Crimson/XS24

The Crimson/XS24 includes all XS features, plus 24-bitplane color, which is useful for compute-intensive applications requiring full color imaging or solids modeling capability. See Figure 2-3 for an illustration of the XS24 board.

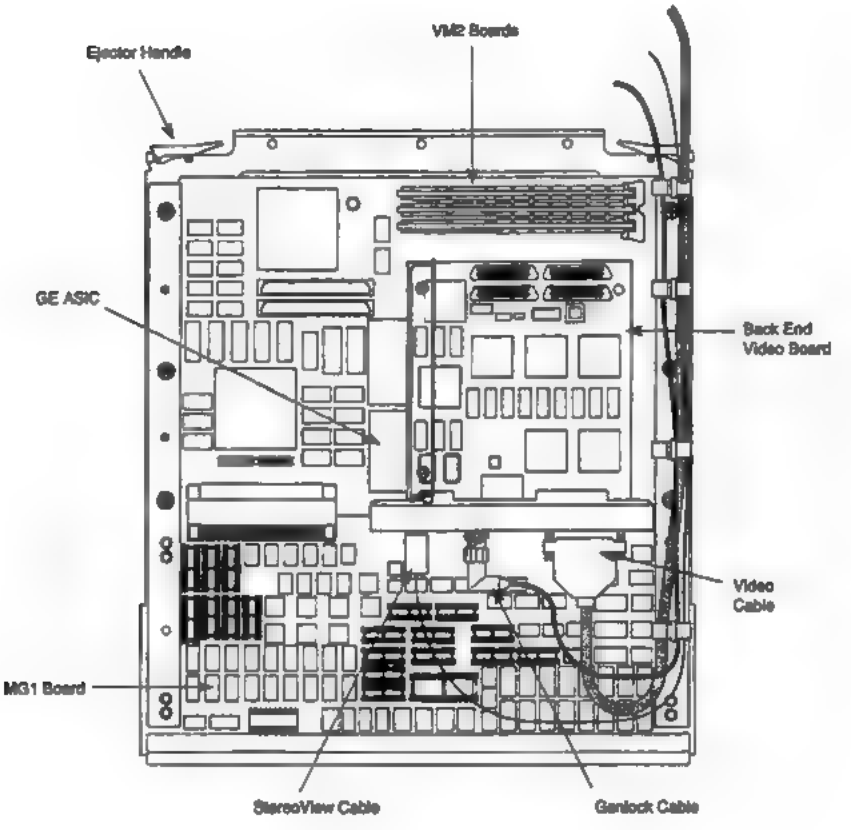


Figure 2-3 XS24 Graphics Board

2.2.4 Crimson/Elan

The Crimson/Elan contains all XS24 features, plus standard z-buffering hardware, and four Geometry Engine processors to increase polygon performance. See Figure 2-4 for an illustration of the Elan graphics board.

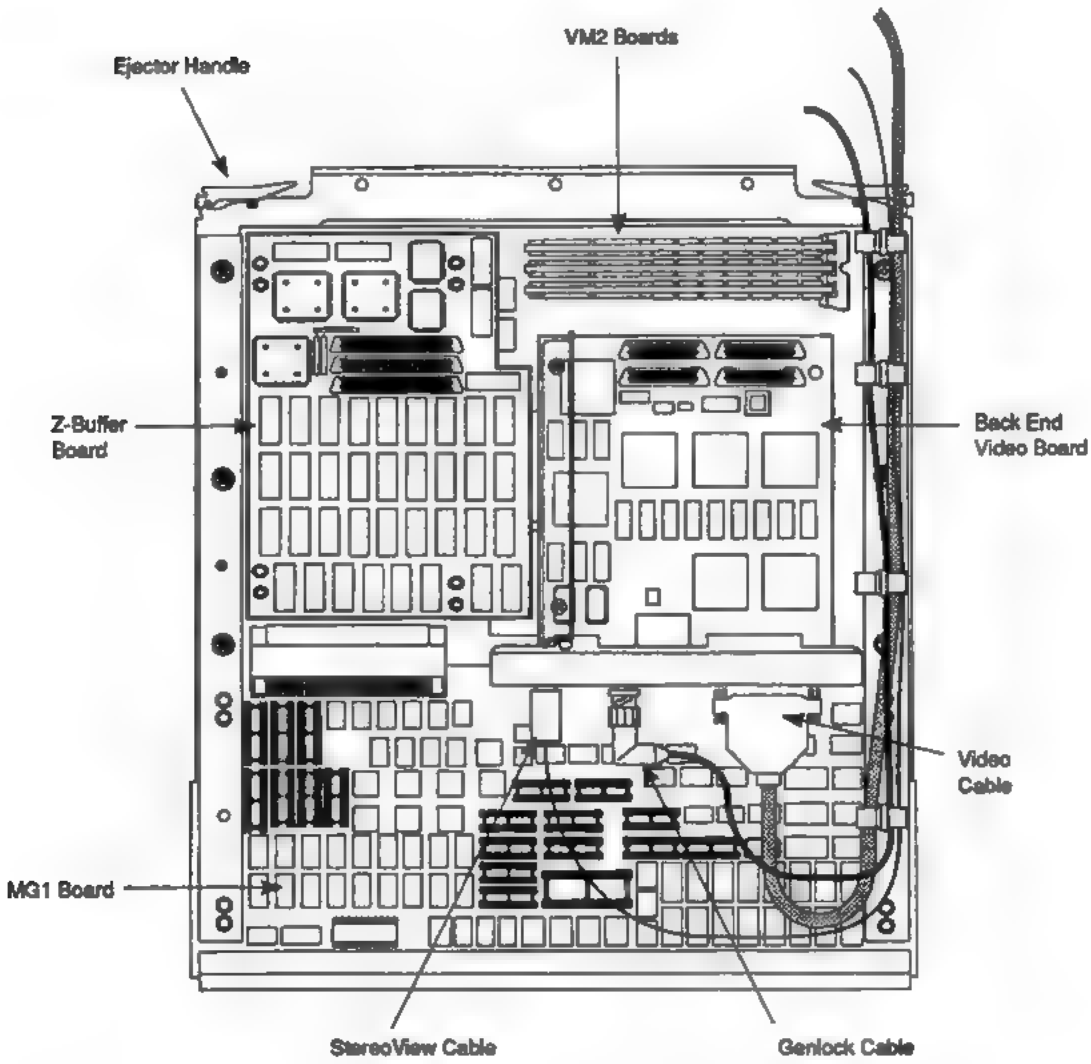


Figure 2-4 Elan Graphics Board

2.2.5 Crimson/VGX

The Crimson/(PowerVision) VGX currently provides the increased polygon performance over the Entry, XS, XS24, and Elan configurations. This four-board set consists of the following:

- one GM3 board
- one GE6 board
- one DGI1 board
- one RM2 board

For additional information on the VGX board set, refer to the *PowerVision Upgrade Installation Instructions* (P/N 007-5391-xxx).

2.2.6 Crimson/VGXT

The Crimson/VGXT includes all VGX features plus higher performance texture mapping made possible by a newer version of the image engine in the RM2 board, the IMP5. The VGX board set uses an IMP3 chip.

For additional information on the VGXT board set, refer to *PowerVision Upgrade Installation Instructions* (P/N 007-5391-xxx) or the *VGXT Installation Instructions* (P/N 108-7013-xxx).

2.2.7 Crimson/Reality Engine

The RealityEngine board set is an enhancement of the PowerVision graphics (VGX/VGXT). The RealityEngine features the following:

- greater texel storage capacity (4 MB versus 256 KB in the PowerVision)
- greater texturing and antialiasing capability
- more color and greater depth and spatial resolution

For further details on the RealityEngine graphics capabilities, see the *RealityEngine Graphics Installation and Configuration Guide* (P/N 108-7036-xxx).

Chapter 3

Site Preparation/Specifications

This chapter defines electrical and environmental requirements and specifications for the Crimson system. Table 3-1 provides system specifications.

3.1 Site Preparation

The following defines preinstallation requirements for the Crimson system.

Caution: The Crimson system requires a NEMA 5–20 amp connector (in the U.S. and Canada) or a NEMA 6–15R amp connector (in Europe and the rest of the world) for proper operation.

3.1.1 U.L. Power Outlet Wiring Requirements

Underwriter Labs (U.L.) requires that the branch circuit wiring be provided with an insulated grounding conductor that is identical in size, insulation material, and thickness to the earthed and unearthed branch-circuit supply conductors. (The grounding conductor should be green, with or without one or more yellow stripes.) This grounding or earthing conductor should be connected to earth at the service equipment or, if supplied by a separately derived system, at the supply transformer or motor-generator set.

The attachment-plug receptacles in the vicinity of the unit or system should all be of an earthing type, and the grounding or earthing conductors serving these receptacles should be connected to earth at the service equipment.

3.1.2 Physical Space Requirements

This section provides suggested servicing area clearances and ventilation parameters.

Servicing Area

You should have adequate clearance around the system to ensure sufficient room for servicing or installing future upgrades. As a rule of thumb, allow about 3 feet (91.44 cm) around the system.

Ventilation

Make sure that all objects are kept at least 12 inches from all sides of the chassis to ensure adequate ventilation.

3.1.3 Thermal Requirements

The air conditioning/heating units at the site must be able to keep the Crimson within the following range:

- 59 to 95 degrees F (15 to 35 degrees C)
- 20 to 80 percent relative humidity (noncondensing)

Note: The system adds about 0.44 ton load to the air conditioning.

Table 3-1 provides additional information on thermal requirements.

Parameter	Characteristics
Dimensions	26" x 21" x 29" (65 cm x 54 cm x 74 cm)
Weight	180 lbs. (82 Kg)
Electrical Requirements	
Input Voltage	104 V to 132 V, or 200 V to 240 V
Input Power	1400 W RMS (max.), 2112 VA (max)
Frequency Range	47 to 63 Hz, 60 Hz
Current	16 amps
Power Consumption	1050 W DC continuous
Connector	NEMA 5–20 amp (U.S. and Canada)
	NEMA 6–15R amp (Europe and the rest of the 220 VAC world)
Safety	
UL	Listed under UL 478 - Data Processing Equipment, Electronic
Canadian Standards Association (CSA)	Certified under CSA 220-M1986 – Information Processing and Business Equipment
TUV	Licensed under CENELEC European Norm EN 60 950/09.87
EMI	FCC Class A, VDE Level A, DOC Class A, VCCI Class 1, CISPR-22, Class 1
Environmental	
Operating	10 to 35 degrees C at sea level
Nonoperating	-40 to +60 degrees C at sea level
Heat dissipation	
- Chassis	4777 BTU/hour max.
- Monitor	512 BTU/hour
Relative Humidity	
- Operating	20 to 80%, noncondensing
- Nonoperating	10 to 80%, noncondensing
Processor	
CPU/FPU	R4000SC (50 MHz external, 100 MHz internal)
Word Length	32/64-bit integer, 64-bit floating point
Operating System	IRIX release 4D1-4.0.3 or later
CPU Memory Size	16 to 256 MB, expandable in 16 or 64 MB increments

Table 3-1 Crimson System Specifications

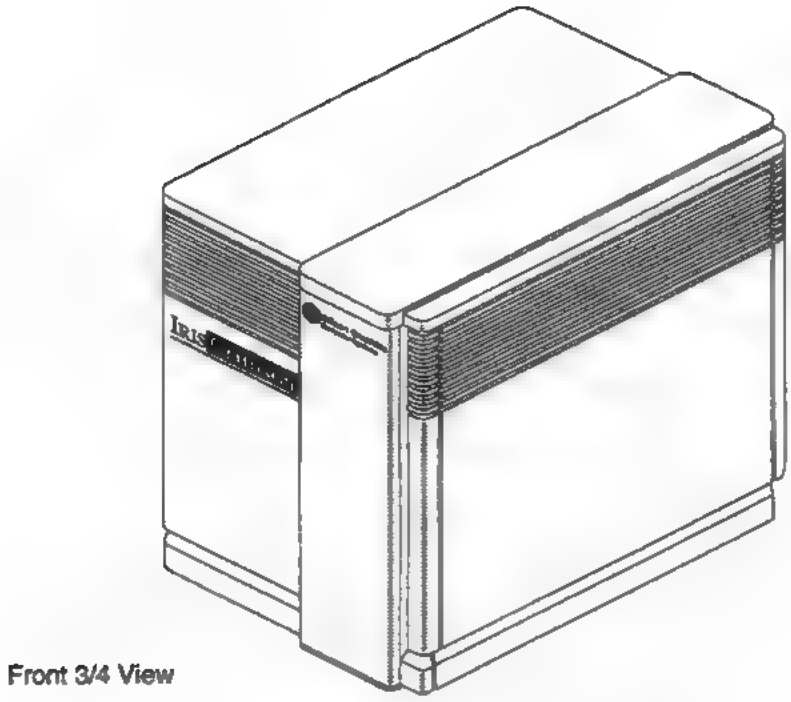
[redacted]	Characteristics
Disk Drive Options	
SCSI	780 MB, 1.2 GB, 1.6 GB
IPI2	1.1 GB
1/4" cartridge	QIC-150 format
8 mm	Helical scan format
4 mm cartridge	DAT format
1/2" reel	800, 1600 6250 bpi, 125 ips
SCSI Ports	Two standard
Serial Ports	Four RS-232 compatible ports (standard), 24 additional ports (optional)

Table 3-1 (continued) Crimson System Specifications

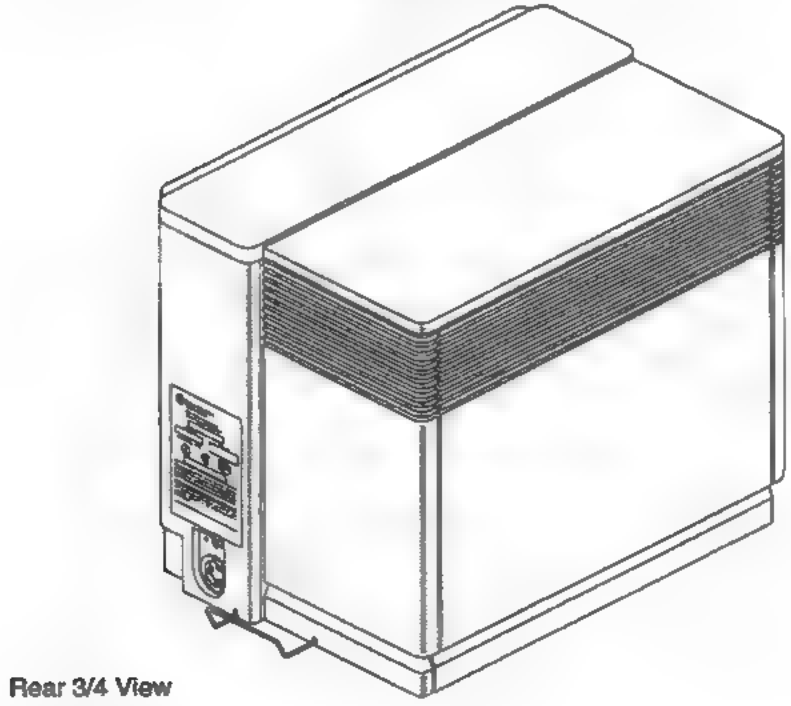
Chapter 4

Chassis Tour

This chapter provides an overview of the IRIS Crimson chassis; a description of the controls, connectors, and indicators; and functional descriptions of the status panel, serial I/O connector board, and the backplane. Figure 4-1 shows the IRIS Crimson chassis.



Front 3/4 View



Rear 3/4 View

Figure 4-1 External View of the IRIS Crimson Chassis

4.1 Controls, Connectors, and Indicators

Figures 4-2 and 4-3 show the locations of the standard controls, connectors, and indicators on the IRIS Crimson chassis, and Tables 4-1 and 4-2 describe each item.

Item	Description
Power Receptacle	This socket accepts a NEMA 120V/20 amp or 220V/15 amp power cable (International systems: 220V/10 amps).
Main Circuit Breaker	This circuit breaker switch controls the main power supply to the chassis and protects the system from electrical damage. The internal power supply fan continues to run for approximately 20 seconds when the circuit breaker is toggled to the OFF position. There are two types of circuit breakers: a 30 amp breaker for the 120 V systems and a 15 amp breaker for 220 V systems.
System Power Switch	This switch controls the supply of DC power to the system. It operates as a secondary switch to the main power circuit breaker. The internal power supply fan is not disabled.
Reset Switch	This switch transmits a hardware reset command to the workstation. It is used only if the workstation does not respond to keyboard or mouse commands.
Power LED	This indicator glows when the System Power Switch is ON and DC power levels are normal.
Fault LED	This indicator glows when software faults are detected.
Thermal or Voltage Circuit Breaker	This circuit breaker interrupts the system power when thermal or voltage limits are exceeded.
Power Status LEDs	This group of LEDs indicates the voltage (and chassis temperature status) of the +5, +12, -5, and -12 DC circuits.
Power DIP Switches	These switches change the power-up test setting.
Status Hexadecimal Display	This LED array displays the system operating status. During normal operation, it alternately flashes 0 and 1.
Keyboard Connector	This 15-pin D-sub connector accepts the ASD keyboard cable.
Ethernet Connector	This connector provides a standard Ethernet connection.
13W3	This output connector replaces the RGB BNC connectors on earlier Silicon Graphics workstations.
Red, Green, Blue BNC Connector	These connectors provide red, green, and blue signals to the standard Silicon Graphics monitor for a Crimson VGX or VGXT system.
SYNC Connector	This BNC connector provides video signal for monitors with external sync. This connector is normally unused with a Silicon Graphics monitor (which obtains sync from the green signal). The SYNC mode is also selectable using the PROM monitor.

Table 4-1 IRIS Crimson Controls, Connectors, and Indicators

Item	Description
Serial and DIN Connector Board	This connector board provides various connectors for system peripherals.
SCSI Connectors	These connectors support external SCSI devices.
SCSI Terminators	These terminators complete a SCSI circuit.
Spare I/O Plates	These plates provide expansion space for options.

Table 4-1 (continued) IRIS Crimson Controls, Connectors, and Indicators

Connector	Function
SVHS	Super VHS. These two electrically separate output channels enable you to connect an SVHS recorder on one port and a monitor on the other port. The channels are interchangeable.
13W3	This output connector replaces the RGB BNC connectors on older workstations.
SYNC	This output connector provides an external sync signal for non-Silicon Graphic monitors, as required.
GEN IN	This input connector allows the system to line-lock to an external video source.
GEN OUT	This output connector enables the master sync source to loop through the system to other equipment.
ALPHA	This connector provides output for transparent or color blending renderings.
CMPST A/CMPST B	CMPST A and B provide a composite video output signal for a recording device and monitor. The channels are interchangeable.
FRAME GRAB	This input connector provides acquisition control.
SWAP READY	This input connector enables multiple systems to be slaved together to provide synchronous frame display.

Table 4-2 IRIS Crimson RealityEngine Connector Functions

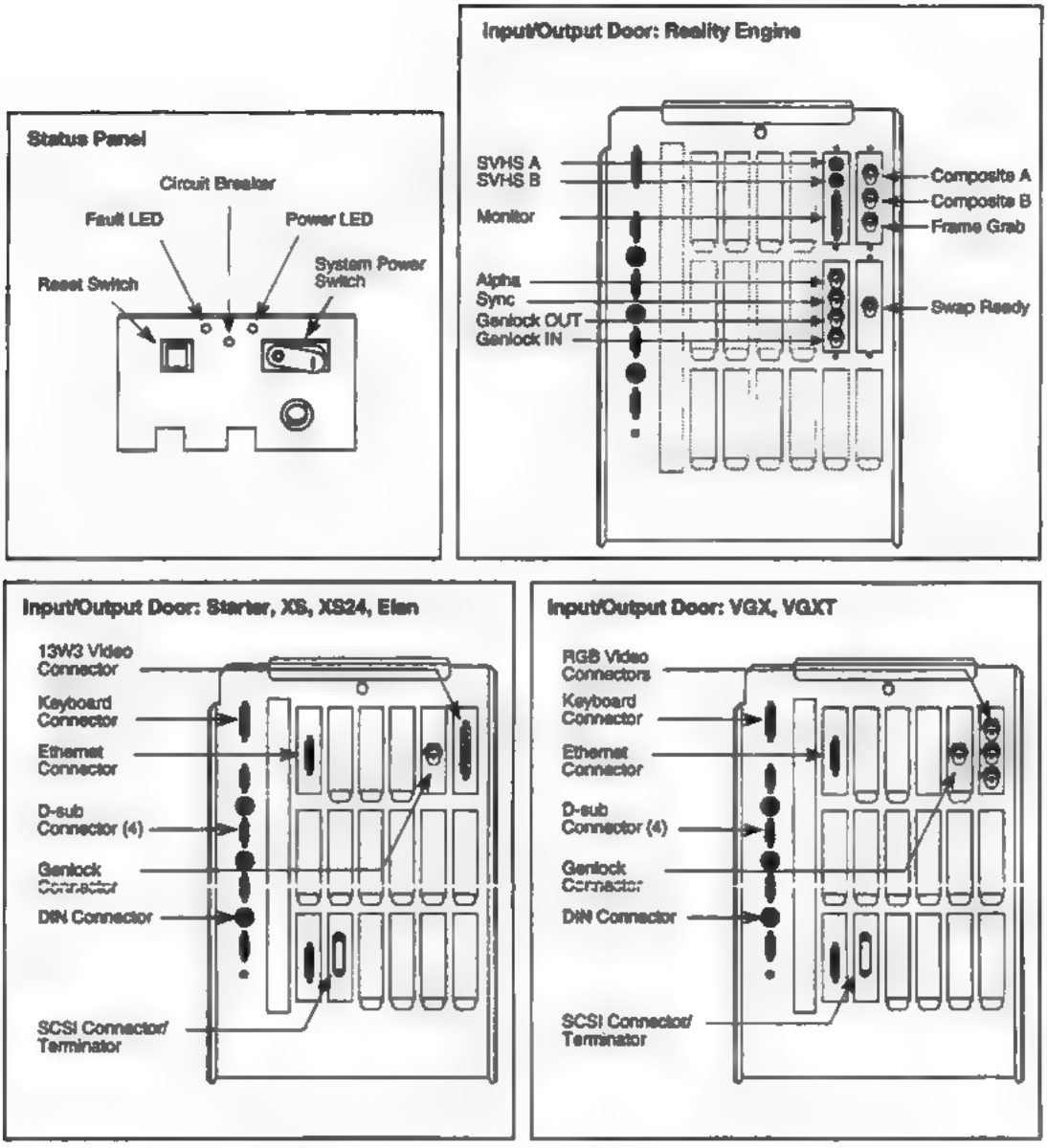


Figure 4-2 Location of Controls, Connectors, and Indicators (Front View)

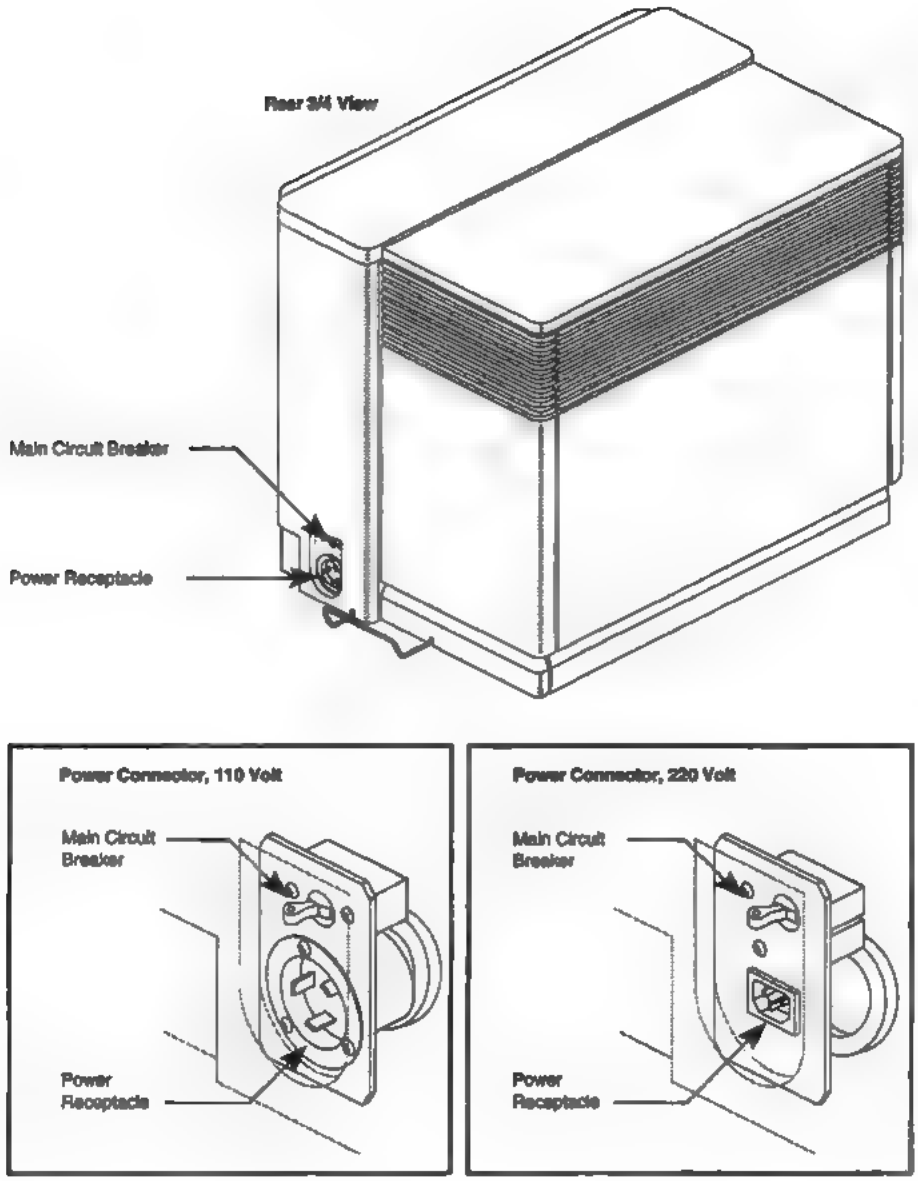


Figure 4-3 Location of Controls, Connectors, and Indicators (Rear View)

4.2 Functional Description

This section provides a functional description of the status panel, serial I/O connector board, and the backplane.

4.2.1 Status Panel (PS3)

The status panel is a PCB assembly of operating controls and indicators. When the status panel is positioned in the chassis, general operating controls and indicators are external, and diagnostic controls and indicators are internal.

External Controls and Indicators

This section provides a description of the external controls and indicators for the Crimson system.

Warning: **This equipment utilizes electrical power internally that is hazardous if the equipment is improperly disassembled. To completely remove power from the system and the power supply, toggle the main circuit breaker to the OFF position and disconnect the power cord.**

System Power Switch
controls the supply of DC power to the system. In certain systems the power supply uses an internal cooling fan that is not connected to the system power switch. This allows the fan to continue running after the system power switch is toggled to the OFF position.

Reset Switch
transmuts a hardware reset command to the workstation. It is used only if the workstation does not respond to keyboard or mouse commands.

Green Run LED
glows continuously when the system power switch is toggled to the ON position and indicates that the DC power levels are normal.

Yellow Fault LED
glows when you toggle the system power switch ON. The LED turns off when the operating system has booted. The yellow fault LED glows continuously when software failures are detected, or when the hexadecimal display shows a number other than 0 or 1.

Thermal or Voltage Circuit Breaker
senses DC voltage level abnormalities or high temperatures within the system; this circuit breaker interrupts the main power. To reset the circuit breaker, press in the triggered plunger; see Figure 4-2 for the plunger's location.

When the exhaust air temperature exceeds 60 degrees C (+/- 5%), the circuit breaker activates. You can reset the circuit breaker once the exhaust air cools to 40 degrees C (+/-5 percent) for one minute or longer.

If any supply voltage drops or rises more than 40 percent, the circuit breaker activates.

Internal Controls and Indicators

This section describes the Crimson internal controls and indicators.

Status Hexadecimal Display
: displays the system operating status. During normal operation, it alternates between 0 and 1.

Power DIP Switches
: control the power-on mode. The system is shipped with all switches in the closed position (see Figure 4-4). The four modes are:

- *Power-on mode* (hex value of 0x81). When the switches are set to this value, the processor drops into the power-on mode. The CPU stack is in the first-level cache in the power-on mode.
- *Debugger mode* (hex value of 0x82). When the switches are set to this value, the PROM drops into the SYMMON mode, which is the CPU debugging tool.
- *NODIAG mode* (hex value of 0x84). When the switches are set to this value, the power-on diagnostic tests are bypassed.
- *MPDEBUG mode* (hex value of 0x88). When the switches are set to this value, the CPU drops into the debugger. The CPU displays the results of the power-on test on tty port 1.

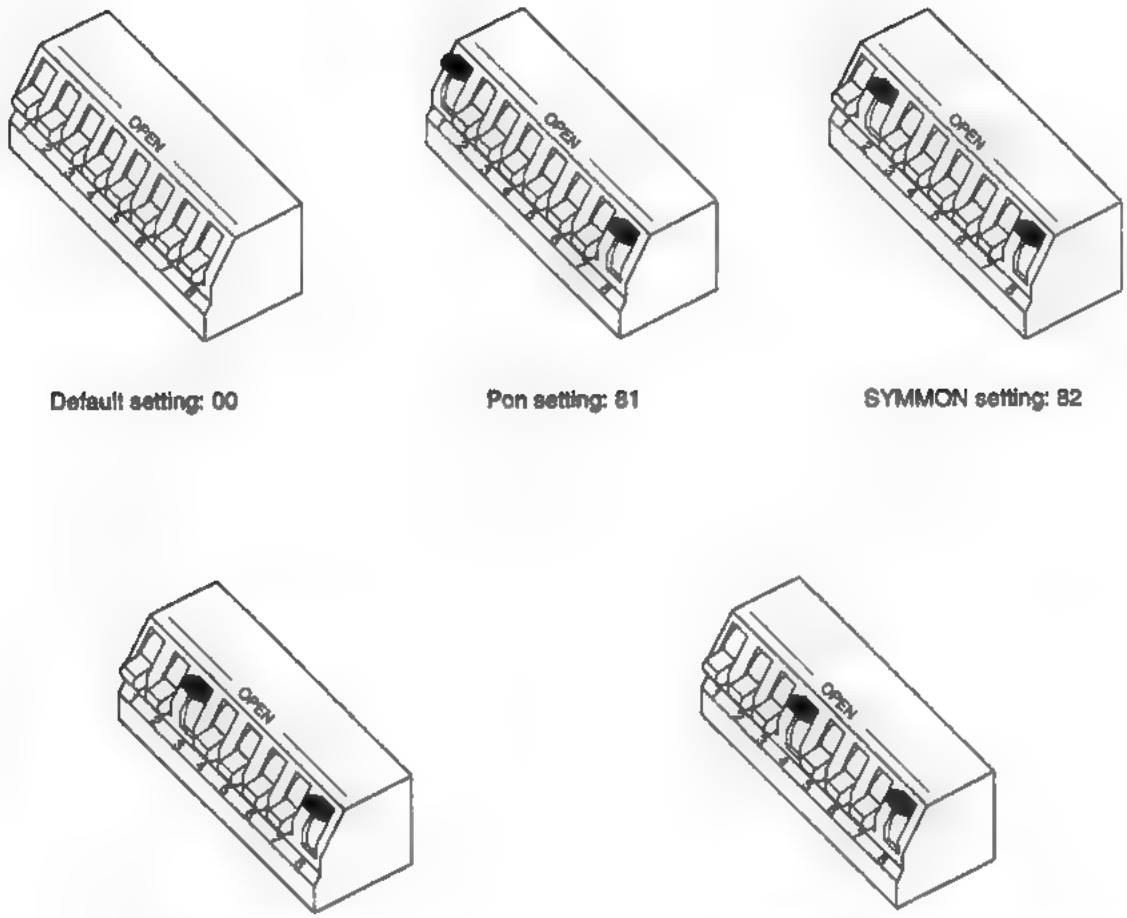


Figure 4-4 Status Panel Power-on Switch Settings

4.2.2 Serial I/O Connector Board (PP2)

The PP2 board is an interface board that mounts on the I/O door and provides an interface between the CPU and system serial peripherals. The board provides signals, power, over-current protection, and EMI filtering on appropriate connectors.

The PP2 provides external and internal connectors. External connectors provide an interface for peripherals, and internal connectors provide interfaces in the chassis.

External Connectors

This section describes the external connectors on the Single Tower and Crimson systems. See Figure 4-2 for the location of these connectors.

Note: The 8-pin and 9-pin connectors are paired together to share common wiring. Hence, only one connector in a pair can be used at a time.

P1 This miniature stereo connector is not currently used.

P2, P4, P6, P8
These 9-pin D-sub connectors provide serial interfaces to terminals and other serial devices. Software assignments for these are */dev/tty[dmf][1234]*, respectively. See Table 4-3 for the pin assignments.

P3, P5, P7 These circular 8-pin DIN connectors provide power and signal interfaces to serial devices. See Table 4-4 for the pin assignments.

P9 This 15-pin D-sub connector provides an interface for the keyboard.

Pin	Assignment
1 and 6	unassigned
2	TXD
3	RXD
4	RTS
5	CTS
7	GND
8	DCD
9	DTR

Table 4-3 9-pin D-sub Connector Pin Assignments

Pin	Assignment
1	DTR
2	CTS
3	Stereo sync
4	RXD
5	TXD
6 and 7	GND
8	+10v

Table 4-4 8-pin DIN Connector Pin Assignments

The Crimson supports four serial ports through the 9-pin D-sub connectors and the circular 8-pin DIN connectors. The four connectors are as follows:

- a connector from P2 or P3
- a connector from P4 or P5
- a connector from P6 or P7
- 9-pin connector P8

Internal Connectors

This section describes the internal connectors in the Crimson system.

J1 This 64-pin header accepts the flat cable that connects the PP2 board to the CPU board for RS232 serial signals.

J2 and J3 These headers provide a "stereo-sync" signal to the PP2 board when the StereoVision option is installed. J2 is a 2-pin header for the RV2 board, and J3 is an 8-pin header.

J4 This header provides +12 volts and -12 volts to the PP2 board.

J5 This header provides the interface for stereo audio signals.

4.2.3 Backplane

The IRIS Crimson chassis uses a 14-slot backplane to provide interconnection and power to the boards in the system. The backplane is integrated into the chassis.

The backplane provides two types of board connectors:

- Slots 1 through 4, 6 through 8, and 10 through 14: three female 96-pin DIN connectors
- Slots 5, 9: one male 560-pin teradyne connector

The backplane provides four distinct bused signal types: VME, MP (Crimson bus), Video (or Graphics), and SCSI.

VME provides VME-specified signals to slots 1 through 4. The P3 connector of each VME slot provides additional power (pin assignments equal the Sun® power specifications). Note that slot 5 for the IO3B board is a 560-pin system board slot. The IO3B board is the channel interface to the VME bus from the Crimson bus.

MP (Crimson)
accommodates the higher bandwidth requirements of the system. These signals are provided to slots 5 through 9. Note that slot 9 is a 560-pin system board slot; this slot provides the interconnection between the MP bus and the Video bus.

Video accommodates the higher bandwidth requirements between graphics boards. The signals are provided to slots 9 through 14. Slot 9 receives the video signals to provide an interconnection between the MP bus and the Video bus.

SCSI provides SCSI signals for control of SCSI devices. The signals are provided at slot 5 from the IO3B board and to a 50-pin connector on the bottom of the backplane.

4.3 Slot Designations

See Tables 4-5 through 4-8 and Figures 4-5 through 4-8 for information on Crimson board slot locations.

Slot	Slot Type
Slot 1	Optional VME board
Slot 2	Optional VME board
Slot 3	Optional VME board
Slot 4	Optional VME board
Slot 5	IO3B board
Slot 6	IP17 CPU board
Slot 7	Unused
Slot 8	Unused
Slot 9	Unused
Slot 10	Unused
Slot 11	Unused
Slot 12	Unused
Slot 13	Unused
Slot 14	Unused

Table 4-5 Crimson/Server Board Locations

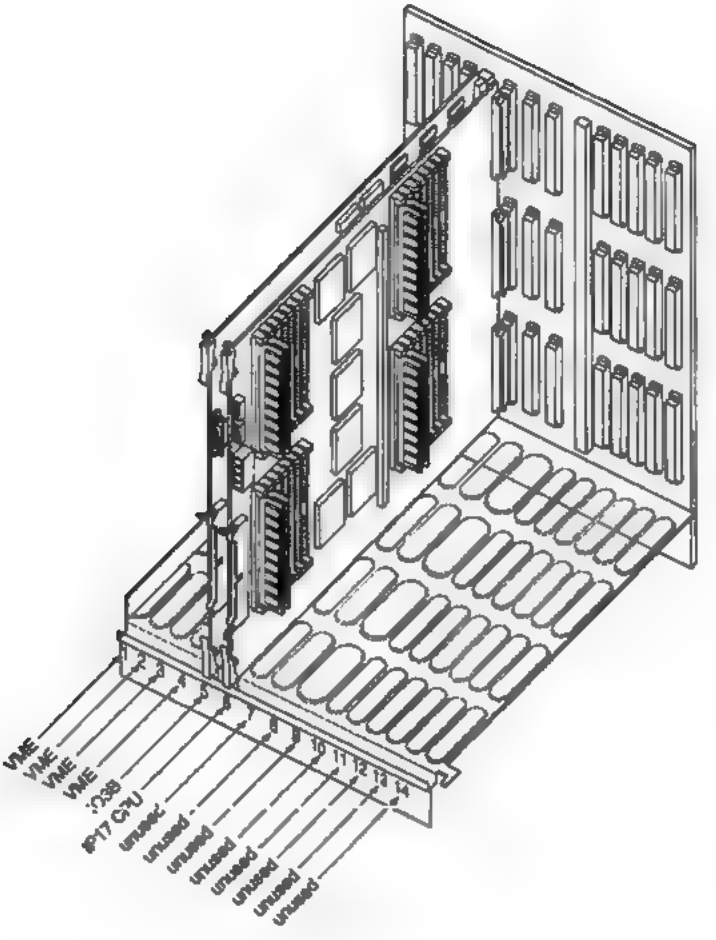


Figure 4-5 Crimson/Server Board Designations

Slot	[redacted] Type
1	Optional VME board
2	Optional VME board
3	Optional VME board
4	Optional VME board or CG3
5	IO3[redacted] board
6	IP17 CPU board
7	Unused
8	Unused
9	Entry, XS, XS24, or Elan boards
10	Unused
11	Unused
12	Unused
13	Unused
14	Unused

Table 4-6 Crimson/Entry, XS, XS24, and Elan Board Locations

Slot	Slot Type
1	Optional VME board
2	Optional VME board
3	Optional VME board
4	Optional VME board or CG3
5	IO3B board
6	IP17 CPU board
7	Unused
8	Unused
9	GM3 board
10	GE6 board
11	Optional video board
12	RM board
13	RM board
14	DG1 board

Table 4-7 Crimson/VGX or VGXT System Board Locations

Note: Refer to the *VO1 Installation Instructions* (P/N 108-7005-xxx) for board slot location information when installing a VO1 board into a Crimson/VGX or VGXT system.

Slot	Slot Type
1	Optional VME board
2	Optional VME board
3	Optional VME board
4	Optional VME board or CG3
5	IO3B board
6	IP17 CPU board
7	Unused
8	Unused
9	GE8 board
10	DG2 board
11	Not currently used
12	RM4 board
13	Not currently used
14	RM4T

Table 4-8 Crimson/RealityEngine Board Locations

Caution: The Crimson does not currently support a 20-span (four RM boards) configuration due to the limitations of the 1050 W power supply.

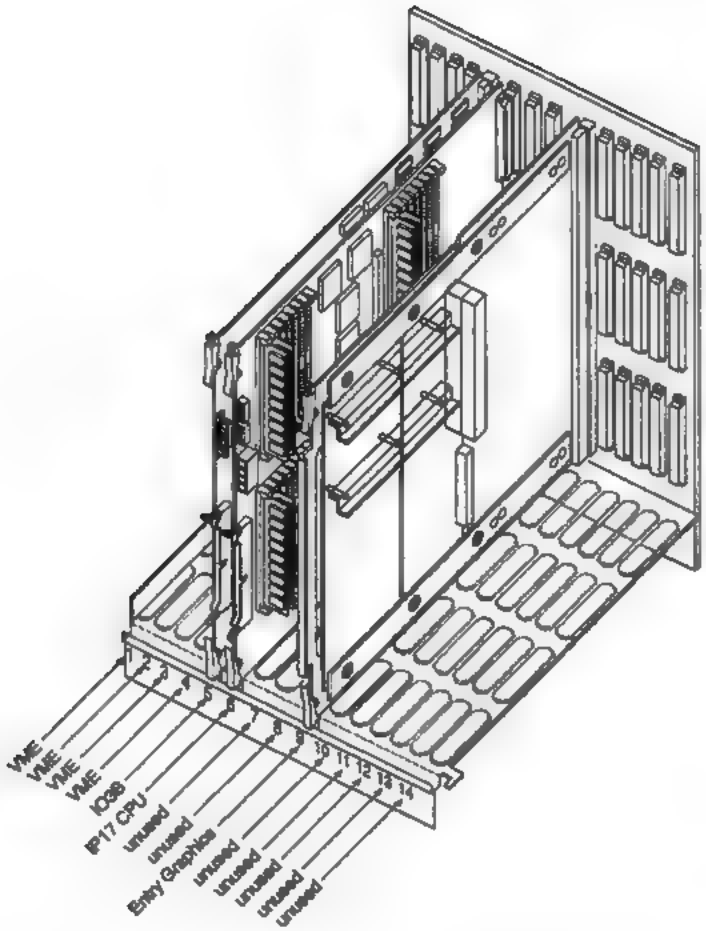


Figure 4-6 Crimson/Entry, XS, XS24, and Elan Board Designations

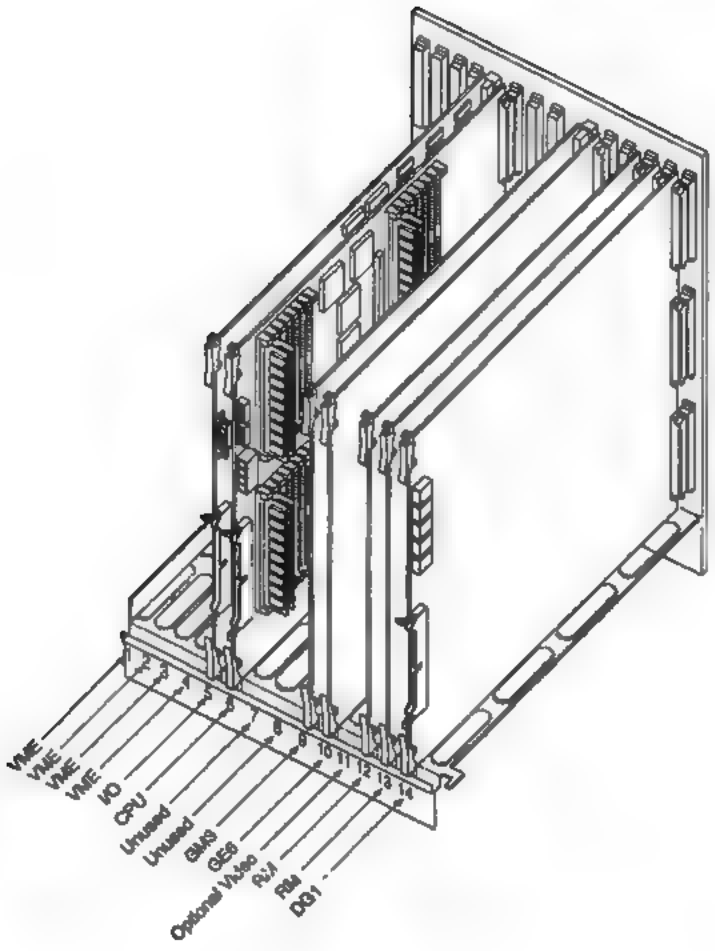


Figure 4-7 Crimson/VGX or VGXT Board Designations

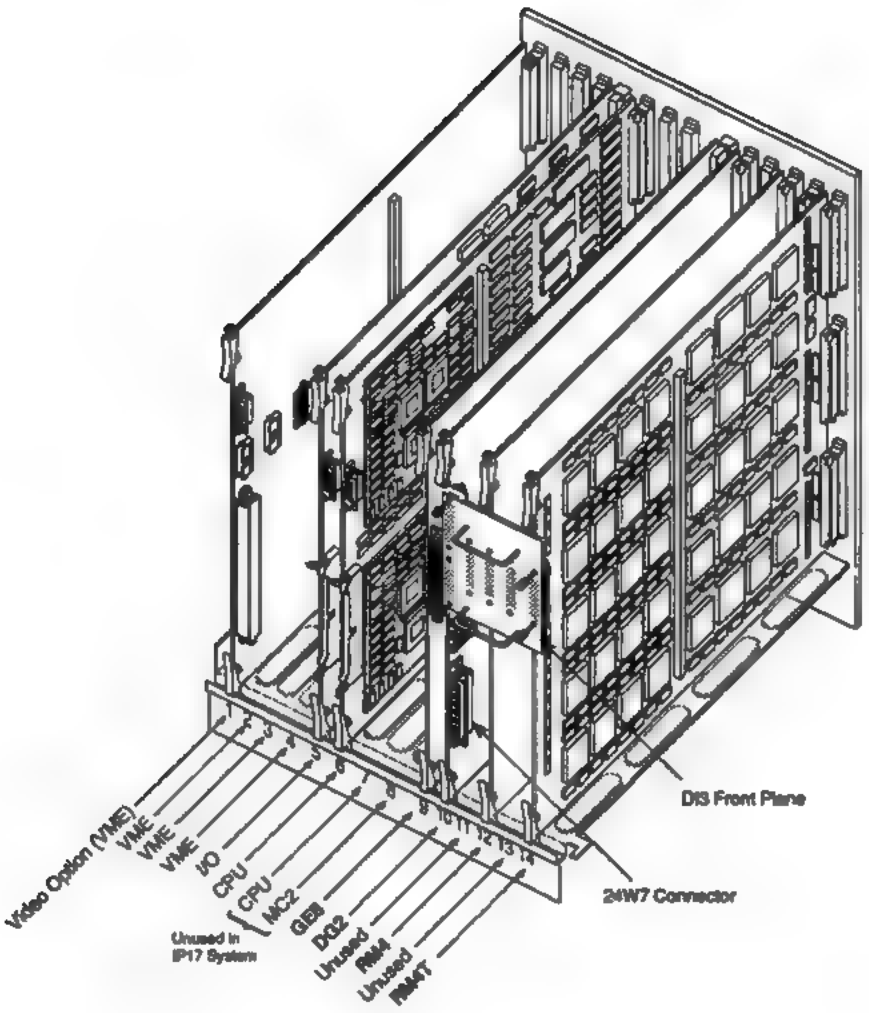


Figure 4-8 Crimson/RealityEngine Board Designations

Chapter 5

Installation

This chapter describes how to install and set up the IRIS Crimson system.

5.1 General Procedures

Depending on the system configuration, you may need to perform one or more of the following tasks before powering up the system:

- load single in-line memory modules (SIMMs) on the IP17 CPU board
- install the MG1/graphics board
- reconfigure the IO3B SCSI cabling
- install peripheral devices
- install option boards
- install a monitor or ASCII terminal

Note: Silicon Graphics ships the Crimson VGX(T) and Crimson RealityEngine systems with the graphics board set already installed.

Note: The fans in the Crimson RealityEngine configuration are set to run on high-speed due to the additional heat dissipation from the graphics board set. The system will generate more noise as a result.

5.2 Loading Memory SIMMs on the IP17

Follow these steps to load memory modules on the IP17 board as required:

1. Open the front door and the I/O door on the chassis as shown in Figures 5-1 and 5-2.

   Note: The door can be removed for easier access to the chassis. To do so, lift up on the door and pull it up from the bottom.

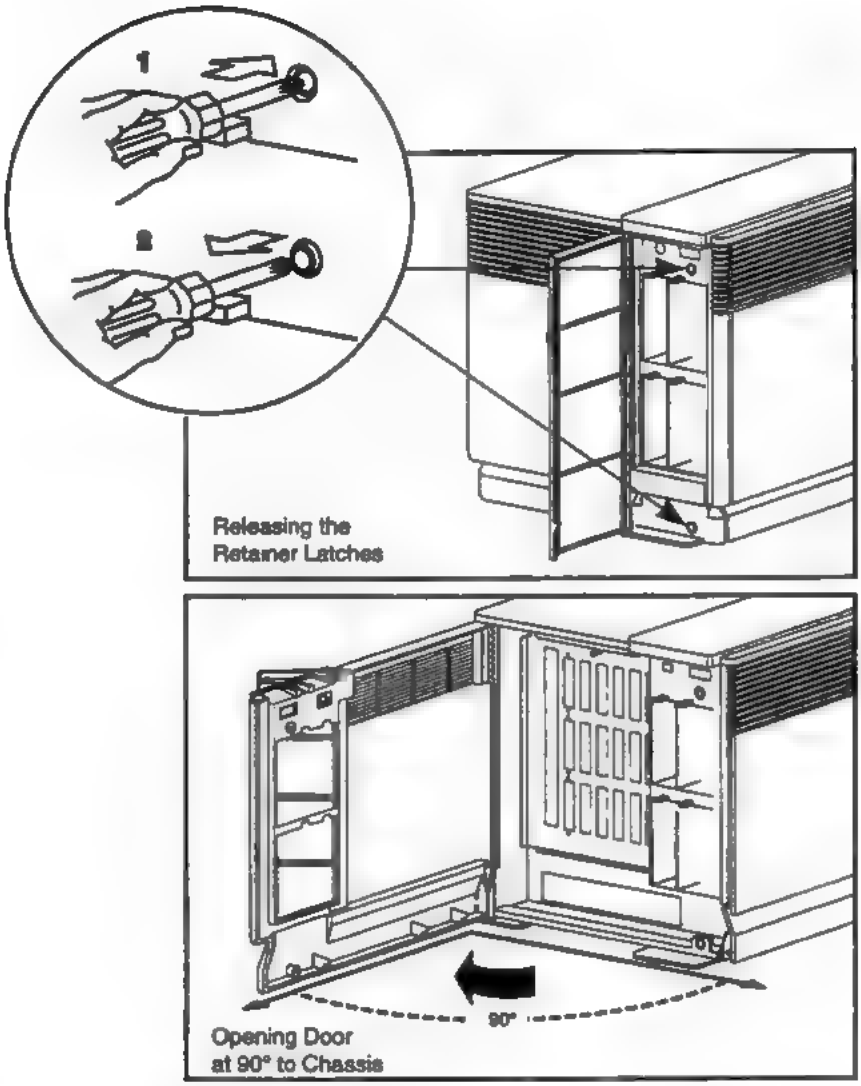


Figure 5-1 Opening the Front Door

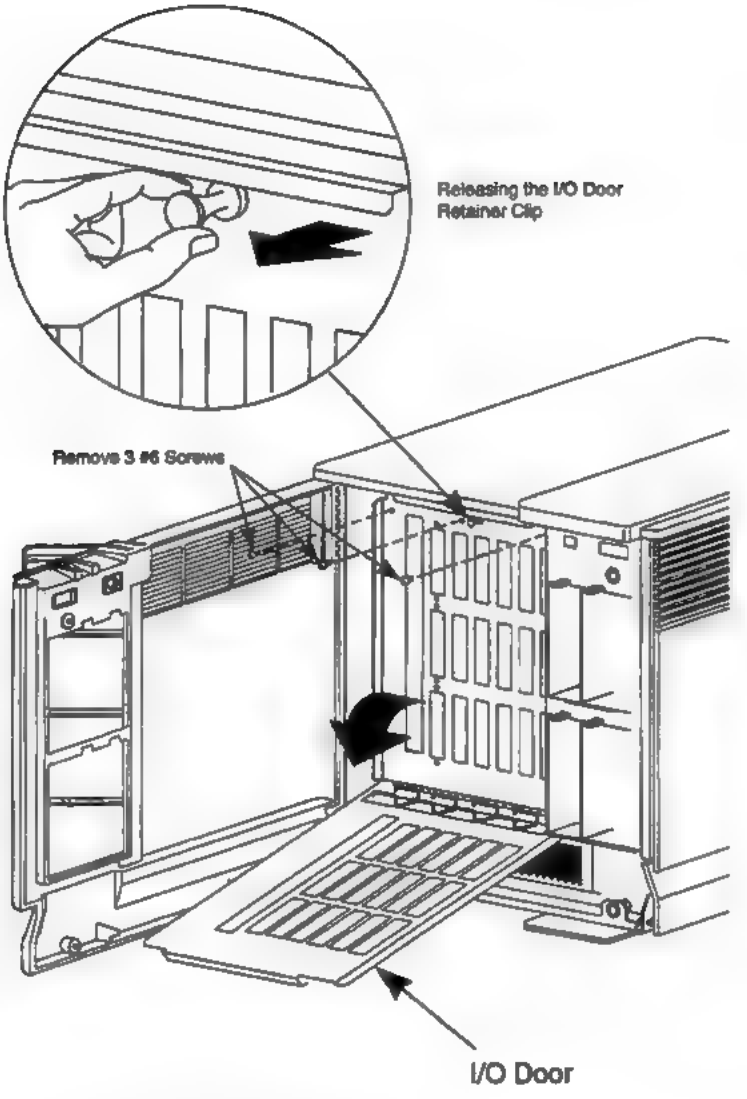


Figure 5-2 Opening the I/O Door

Caution: Be sure you are wearing your ESD ground strap. Disconnect all applicable cable connectors to the I/O panel before removing the boards from the chassis.

2. Disconnect the 64-pin serial I/O ribbon cable connector from the IP17 board. Disconnect the I/O cables from the boards.
3. Use the board ejector tabs to remove the CPU board from the chassis and place it on an antistatic mat.

5.2.1 IP17 SIMM Configuration

SIMMs must be installed in the correct configuration. Refer to the following paragraphs to correctly configure the memory of your IP17 board.

SIMM Blocks and Banks

The IP17 board has 32 SIMM sockets organized into four groups, or blocks. All four blocks are identical. Each block consists of eight SIMM sockets, and every two sockets compose a single bank. There are four banks in each SIMM block (see Figure 5-3).

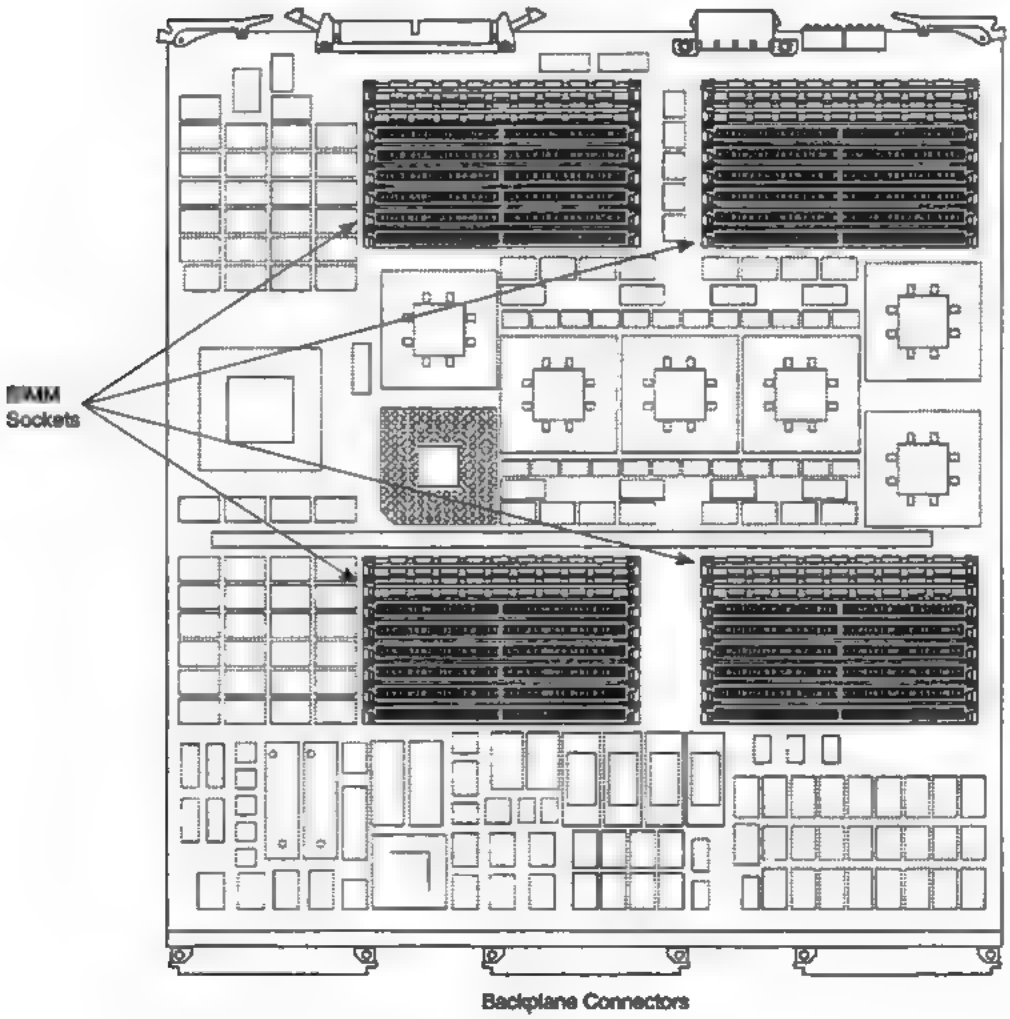


Figure 5-3 SIMM Blocks and Sockets

Allowable SIMM Combinations

When SIMMs are loaded onto the board, bank 1 in each block must be filled first. SIMMs must be installed in groups of eight, as shown in Figure 5-4.

Note: All eight SIMMs in a given location must be of the same type, either high-density or low-density. When the system diagnostics are invoked, only one of the eight SIMMs in a given location is verified. If high-density and low-density SIMMs are mixed, memory errors occur.

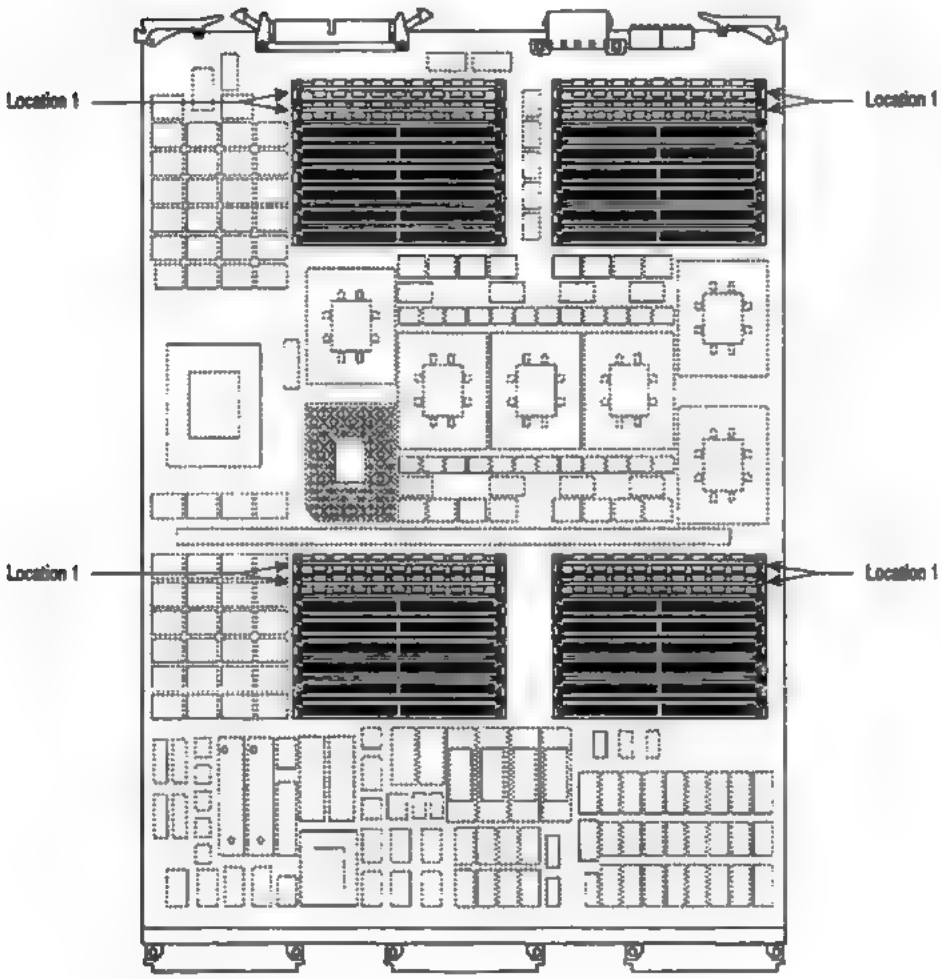


Figure 5-4 Location of SIMM Bank 1 on IP17 Board

The high-density SIMMs contain 8 MB each and are installed 64 MB at a time (8 SIMMs times 8 MB/SIMM). Low-density SIMMs contain 2 MB each and are installed 16 MB at time (8 SIMMs times 2 MB/SIMM). High-density and low-density SIMMs can

be combined on the same block, but only when the high-density SIMMS are installed in the lowest numbered banks (see Table 5-1).

Fourteen different combinations of high-density and low-density SIMMs can be loaded on an IP17 board. These combinations are shown in Figures 5-5 through 5-8. They are also described in Table 5-1.

Note: Before the SIMMs can be installed, you must remove the IP17 board and IO3B board (for jumpering) from the Crimson chassis. The IP17 board resides in slot 6 and the IO3B is in slot 5.

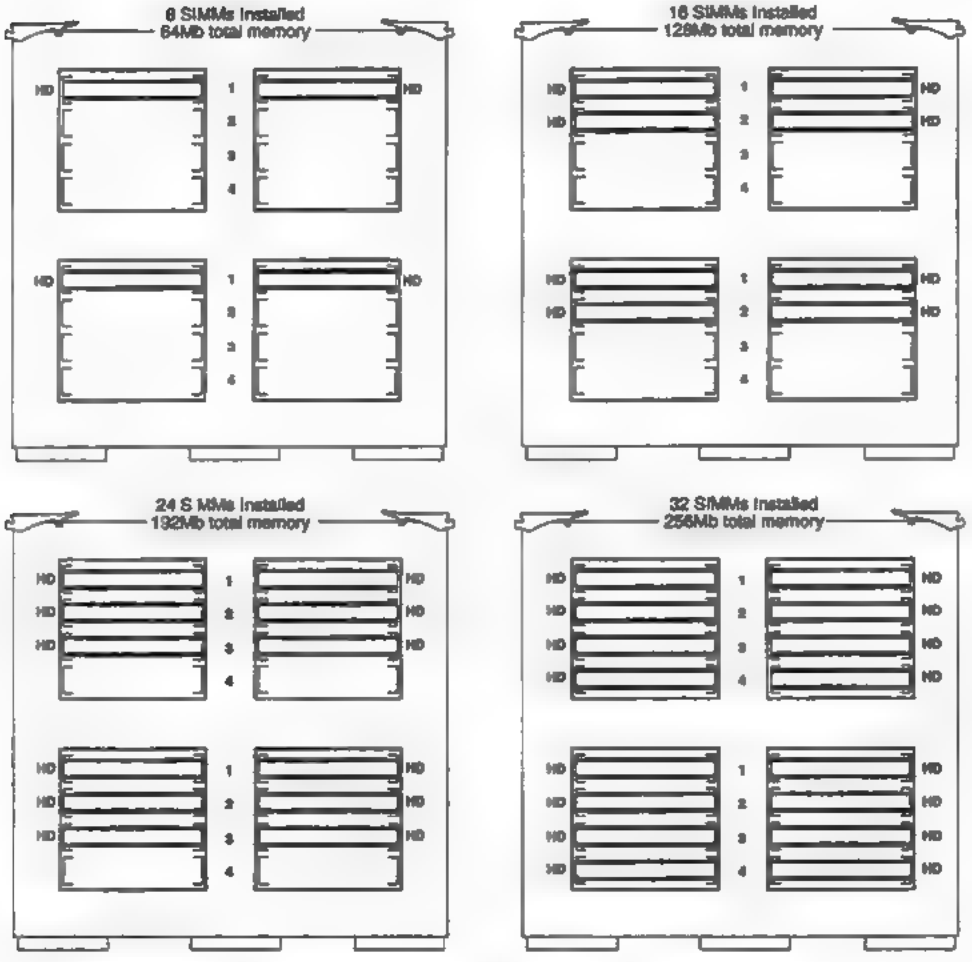


Figure 5-5 High-density SIMM Combinations on the IP17 Board

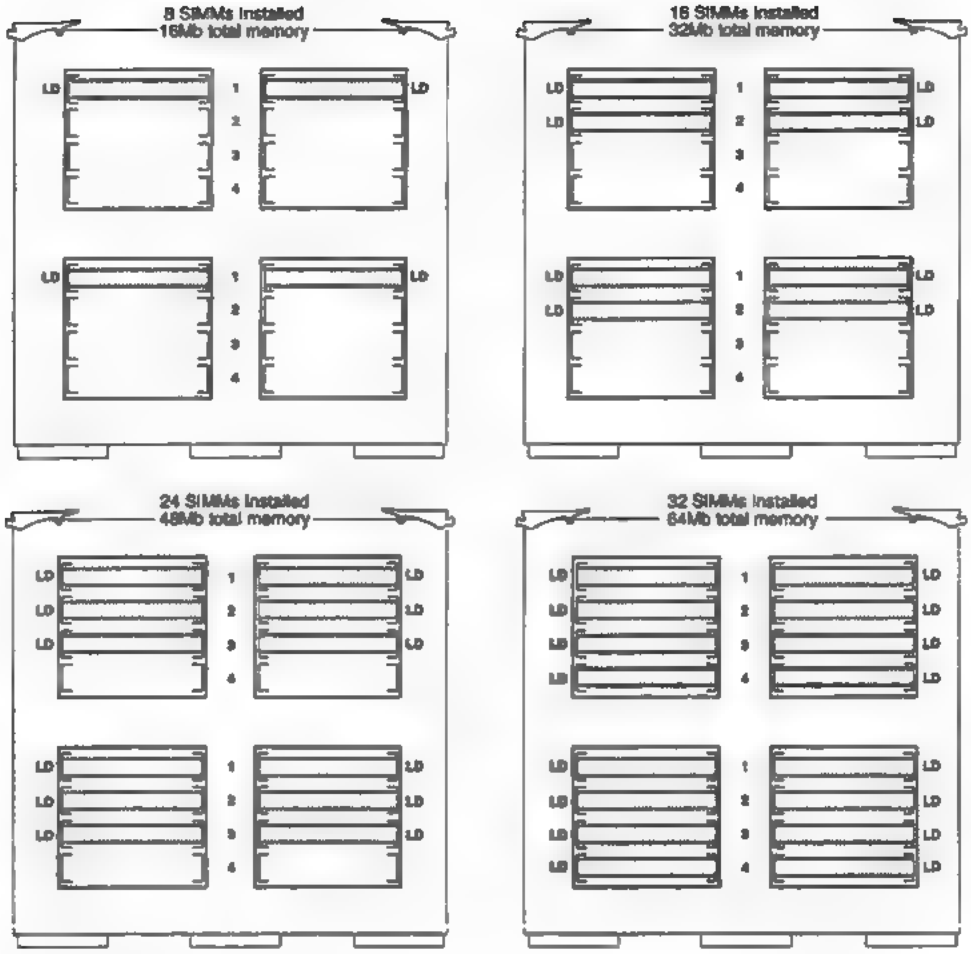


Figure 5-6 Low-density SIMM Combinations on the IP17 Board

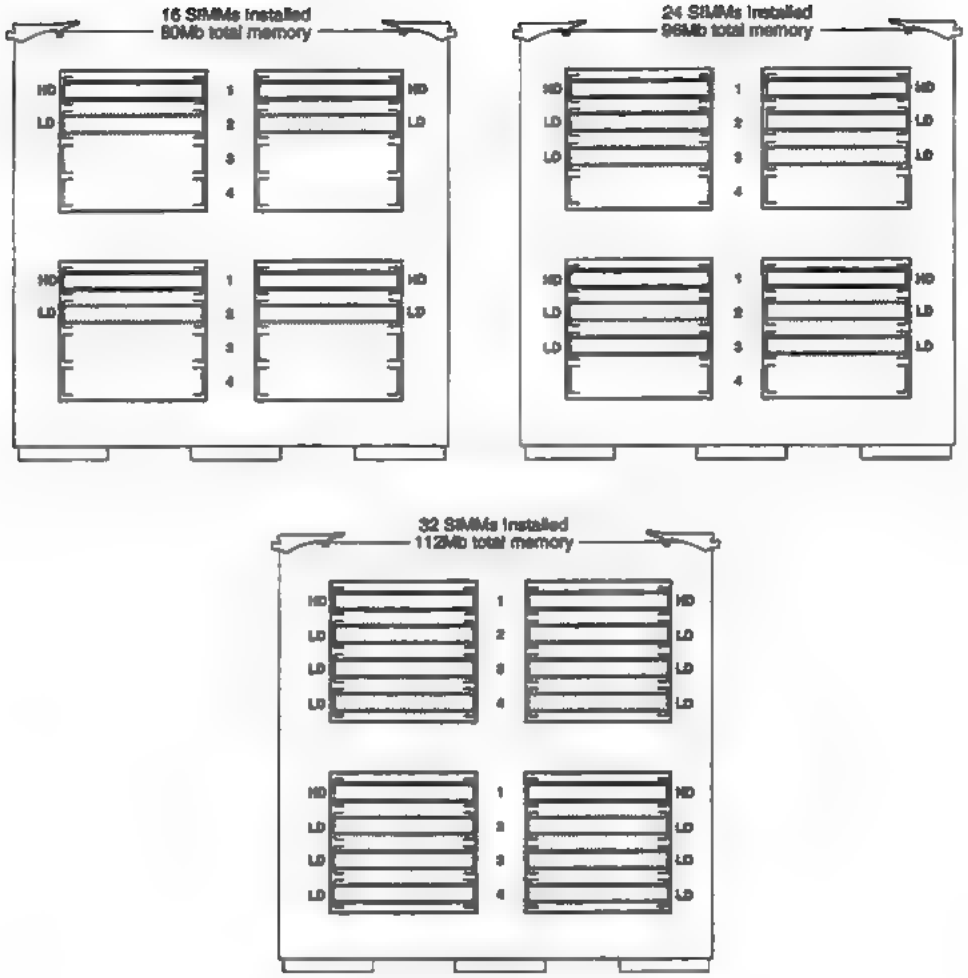


Figure 5-7 High- and Low-density SIMM Combinations on the IP17 Board

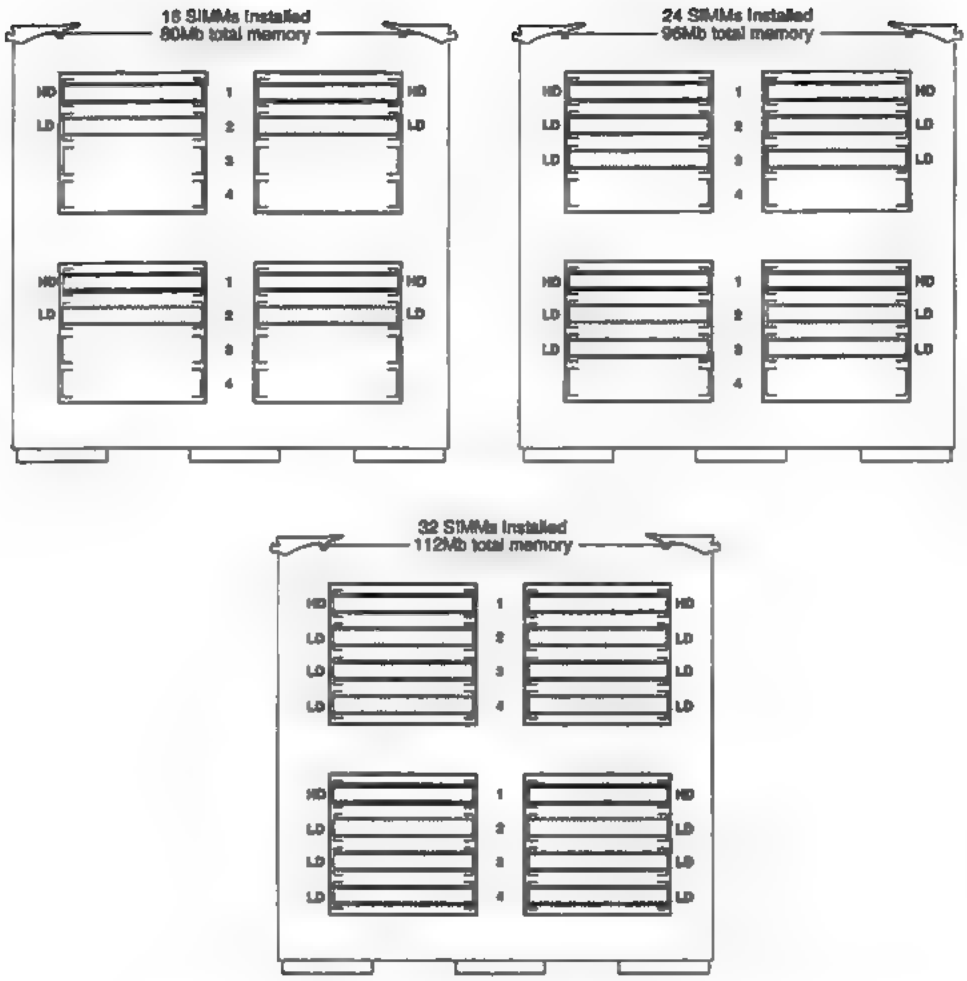


Figure 5-8 High- and Low-density SIMM Combinations on the IP17 Board

Number of SIMMs Installed	SIMM Location 1	SIMM Location 2	SIMM Location 3	SIMM Location 4	Total Memory Installed
8	L-Density	—	—	—	16 MB
16	L-Density	L-Density	—	—	32 MB
24	L-Density	L-Density	L-Density	—	48 MB
32	L-Density	L-Density	L-Density	L-Density	64 MB
8	H-Density	—	—	—	64 MB
16	H-Density	H-Density	—	—	128 MB
24	H-Density	H-Density	H-Density	—	192 MB
32	H-Density	H-Density	H-Density	H-Density	256 MB
16	H-Density	L-Density	—	—	80 MB
24	H-Density	L-Density	L-Density	—	96 MB
32	H-Density	L-Density	L-Density	L-Density	112 MB
24	H-Density	H-Density	L-Density	—	144 MB
32	H-Density	H-Density	L-Density	L-Density	160 MB
32	H-Density	H-Density	H-Density	L-Density	208 MB

Table 5-1 Allowable SIMM Locations on the IP17 Board

Installing the SIMMs

Use the following instructions to install SIMMs on the IP17 board. Install eight SIMMs at a time, two in each corresponding SIMM location in each SIMM block; refer to Figures 5-5 through 5-8 for the proper locations.

1. Slide each SIMM module into a single SIMM location at an angle, with the notch to your right.
2. Gently rock the module back and forth until the connectors are aligned.
3. Carefully push the module down and away from you until you hear the release tabs click into the locked position.

Refer to Figure 5-9 for details on SIMM installation.

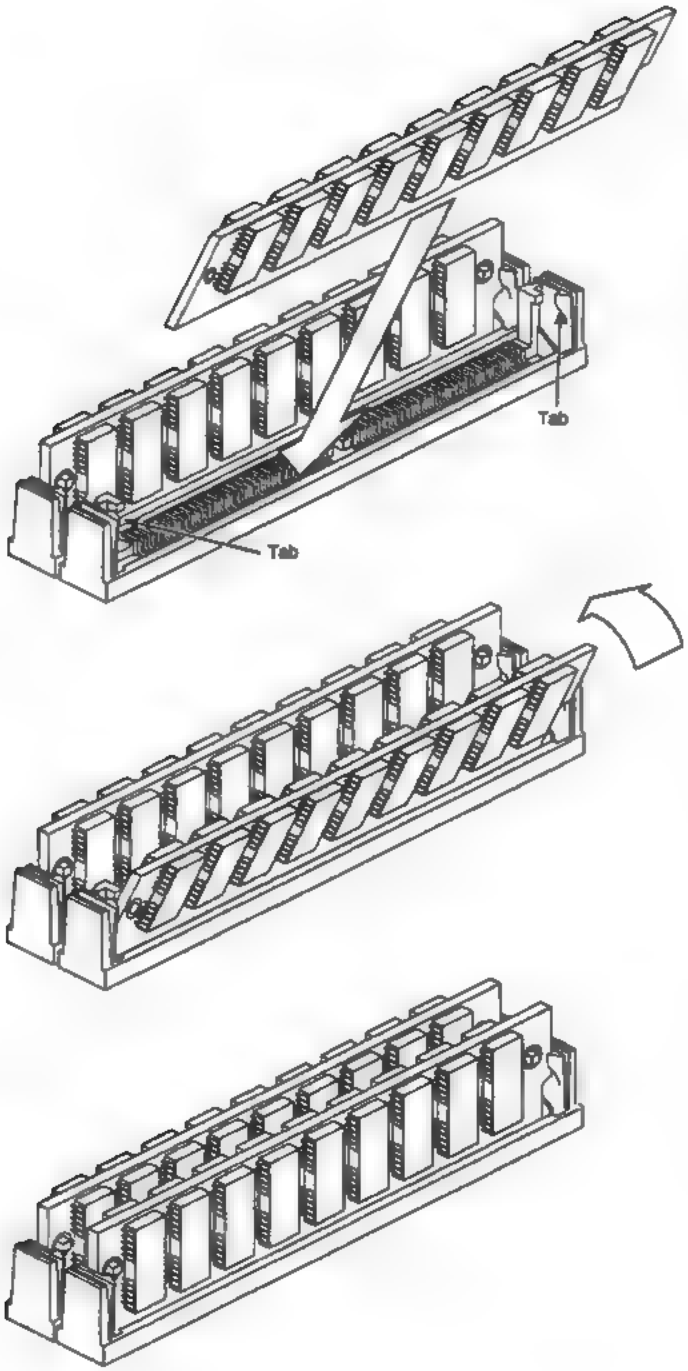


Figure 5-9 SIMM Installation

Jumper on IP17

Verify that the jumper shown in the upper left-hand corner of the board (B0O9) is not installed, see Figure 5-10. If it is installed, remove the jumper now.

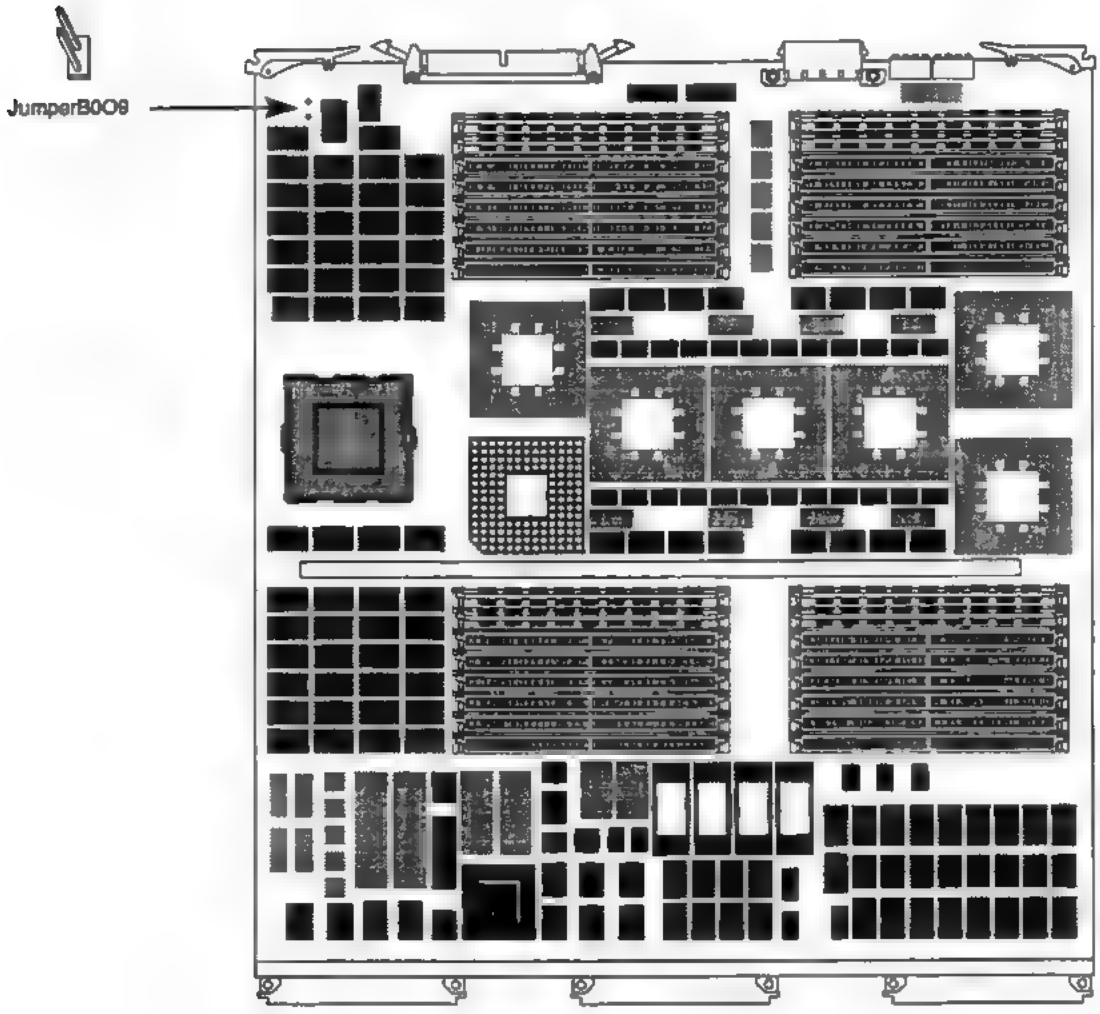


Figure 5-10 IP17 Board Jumper Location

Jumper on IO3B

Verify that the jumper shown in the lower left-hand corner of the board (C0F0) is installed on the pins closest to the backplane connector (Figure 5-11). If it is in the middle location, move the jumper to the end location now.

Note: If the jumper on the IO3B board is not in the correct location, memory errors will occur. In addition, only the IO3B board that comes with this kit will work with the IP17. Do not attempt to use an older version of this board.

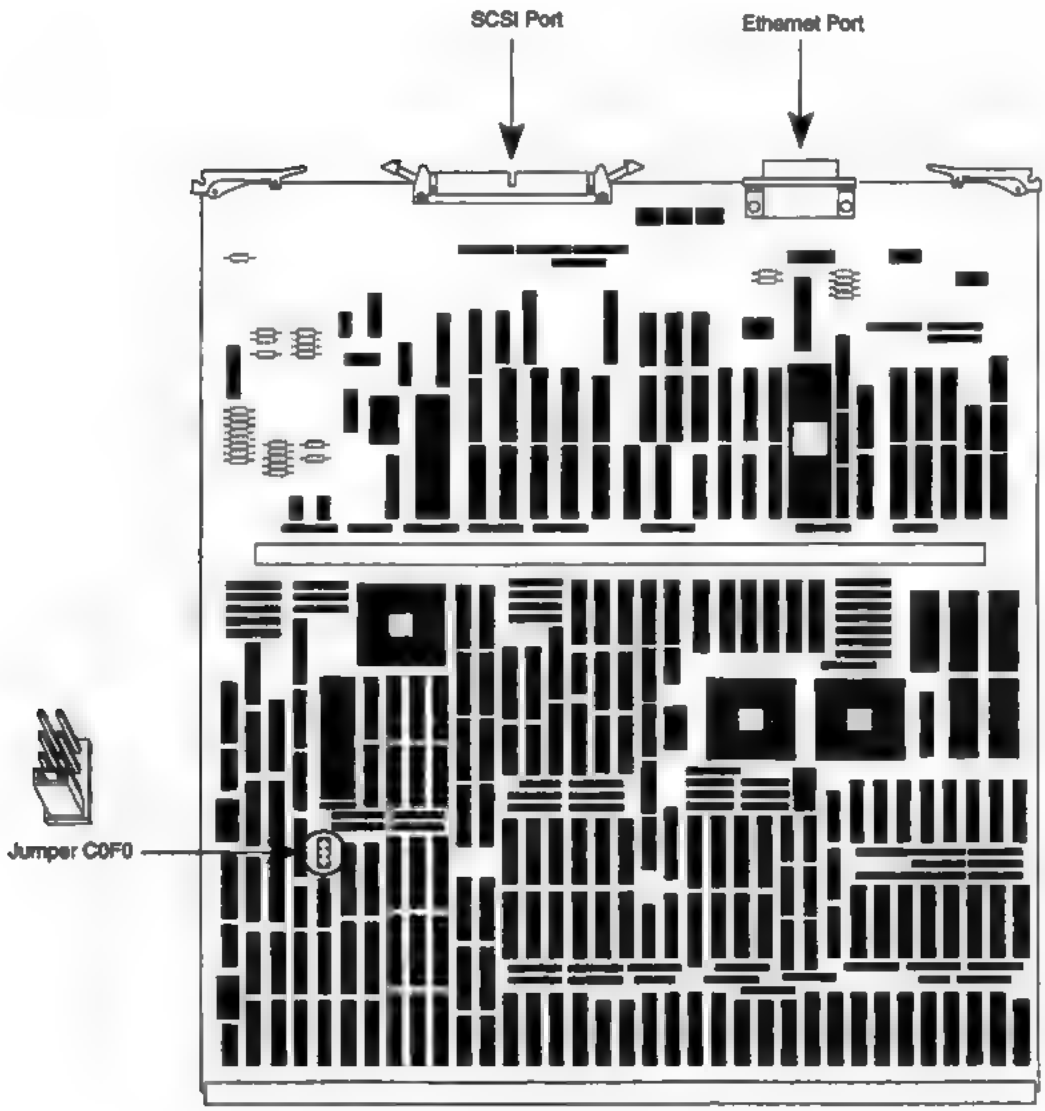


Figure 5-11 IO3 Board Jumper Location

Once all of the available SIMMs are loaded onto the IP17 board and you have verified the jumper locations, you are ready to reinstall the boards. Remember to reconnect any other cables that have been disconnected during this installation.

5.2.2 Installing the MG1/Graphics Board

The MG1/graphics board resides in slot 9 of the chassis. Follow these instructions to install the board into the Crimson system.

Caution: The MG1/graphics board has up to three cable connectors that attach to the graphics hardware. Route these cables through the plastic cable clamps on the board to prevent the cables from chafing against other boards in the system. See Figure 5-12.

1. Ensure that the system is powered down.
2. Open the front and I/O doors.
3. Grasp the MG1/graphics board by the two upper and lower ejector tabs.
4. Place the board in the card guides and slide the card halfway into the chassis. The two rails running along the top and bottom of the chassis act as guides and secure the cards within the chassis.
5. Pull the upper and lower ejector tabs toward you until they line up lengthwise with the horizontal edges of the board.
6. Slide the board completely into the slot while angling the plastic ejectors of the board so that the U-shaped grooves of the ejectors fit into the upper and lower metal frames of the chassis.
7. Push the upper and lower ejector tabs toward the center of the board's lower edge until both lips are vertical. You should hear and feel the board snap into the board ejectors and backplane connectors. The board is now seated in the backplane.

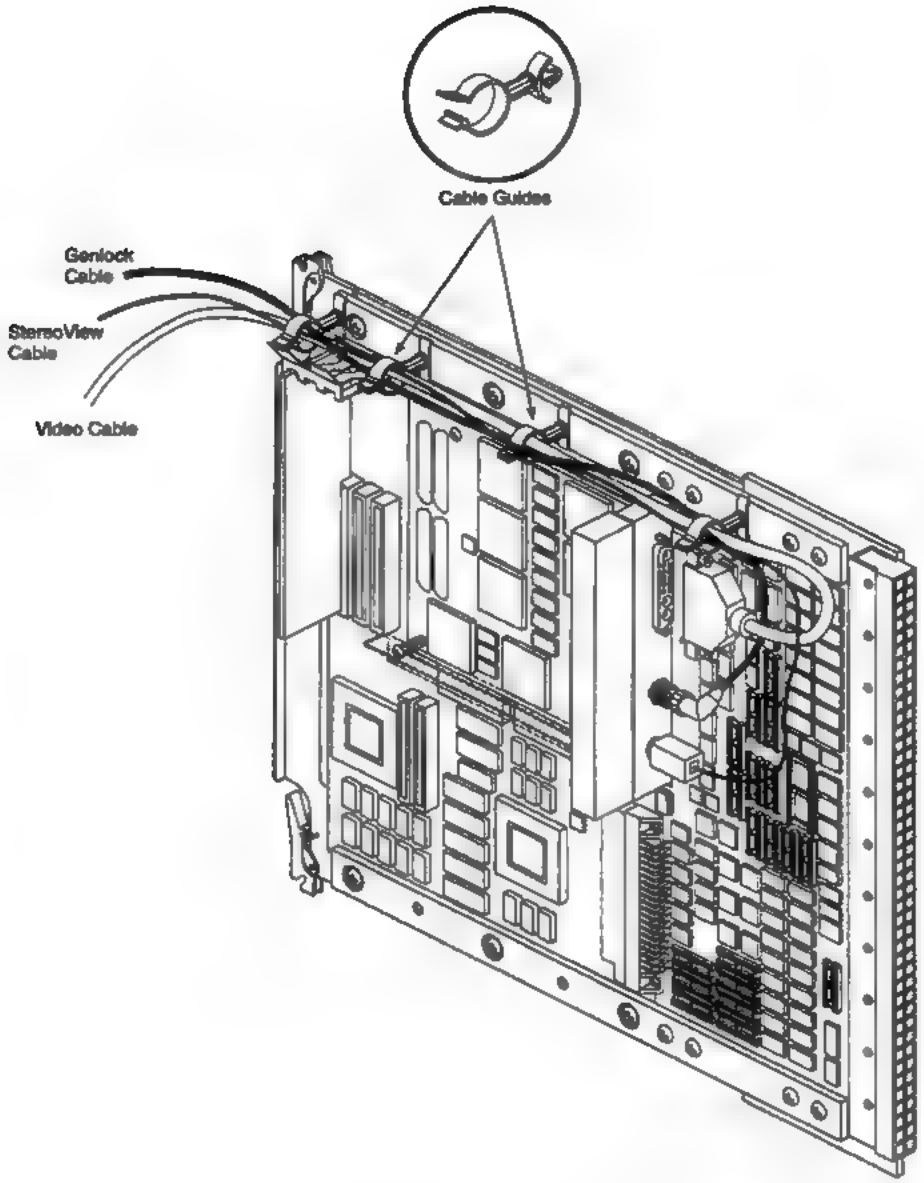


Figure 5-12 MG1/Graphics Board and Cable Connectors

8. Install the cable connectors as follows:
   - install the graphics cable connector to the far right slot on the I/O door. See Figure 5-13.
   - install the SYNC/GENLOCK cable connector (if applicable) to the slot left of the graphics connector. See Figure 5-13.
   - install the stereo-sync connector (for StereoView) to J2 on the PP2 board. See Figure 5-14.

   Note: The Entry system has one cable connector, the 13W3 graphics cable connector. The XS, XS24, and Elan systems have three cable connectors: the graphics cable connector, SYNC/GENLOCK and stereo-sync connector.
9. Close the I/O panel unless there are boards to be installed.

Caution: Remember to disconnect the cable connectors to the I/O panel whenever you remove an MG1/graphics board from the chassis.

5.2.3 Reconfiguring the IO3B SCSI Cables

The standard Crimson system comes cabled with SCSI port 0 of the IO3B board connected to the upper and lower internal drive bays. See Figure 5-15. Port 0 is on the rear of the system. A jumper cable daisy-chains the upper drives to the lower drives. SCSI port 1 of the IO3B is not used in this configuration.

Terminators

The system comes with two terminators. See Figures 5-15 through 5-17 for proper SCSI termination for your system configuration.

Striping the Internal Drives

You may configure the SCSI cabling so that port 0 connects to the lower drive bay and port 1 connects to the upper drive bay. See Figure 5-16. This provides a dedicated channel for each drive bay. This cabling scheme is called *striping*. Striping enables faster I/O throughput. Refer also to the operating system documentation for more information on striping.

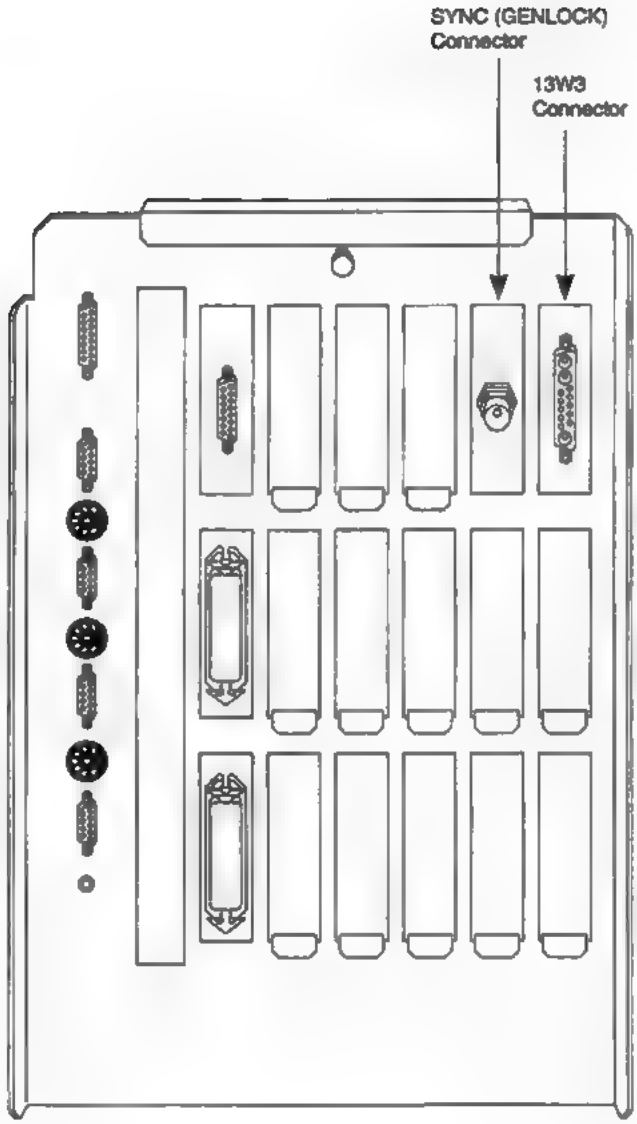


Figure 5-13 Recommended 13W3 Cable and SYNC (GENLOCK) Connector Location

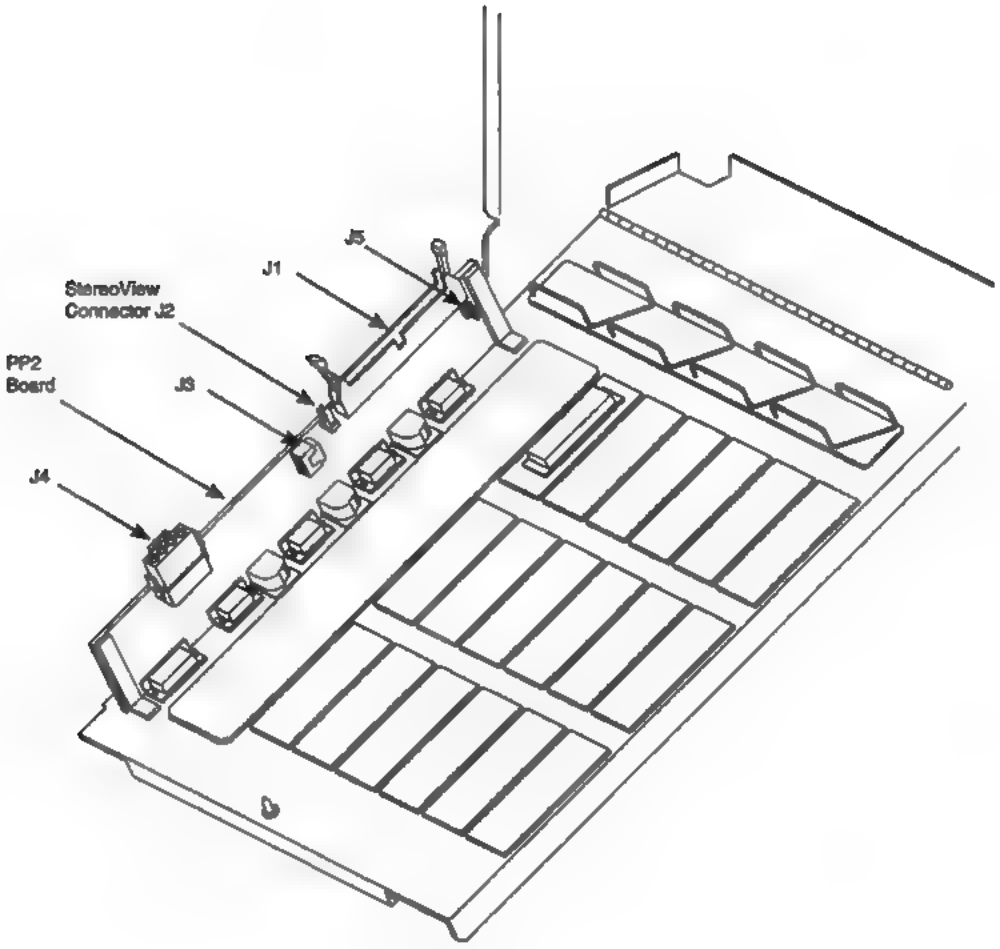


Figure 5-14 Location of StereoView Connector (J2) on PP2 Board

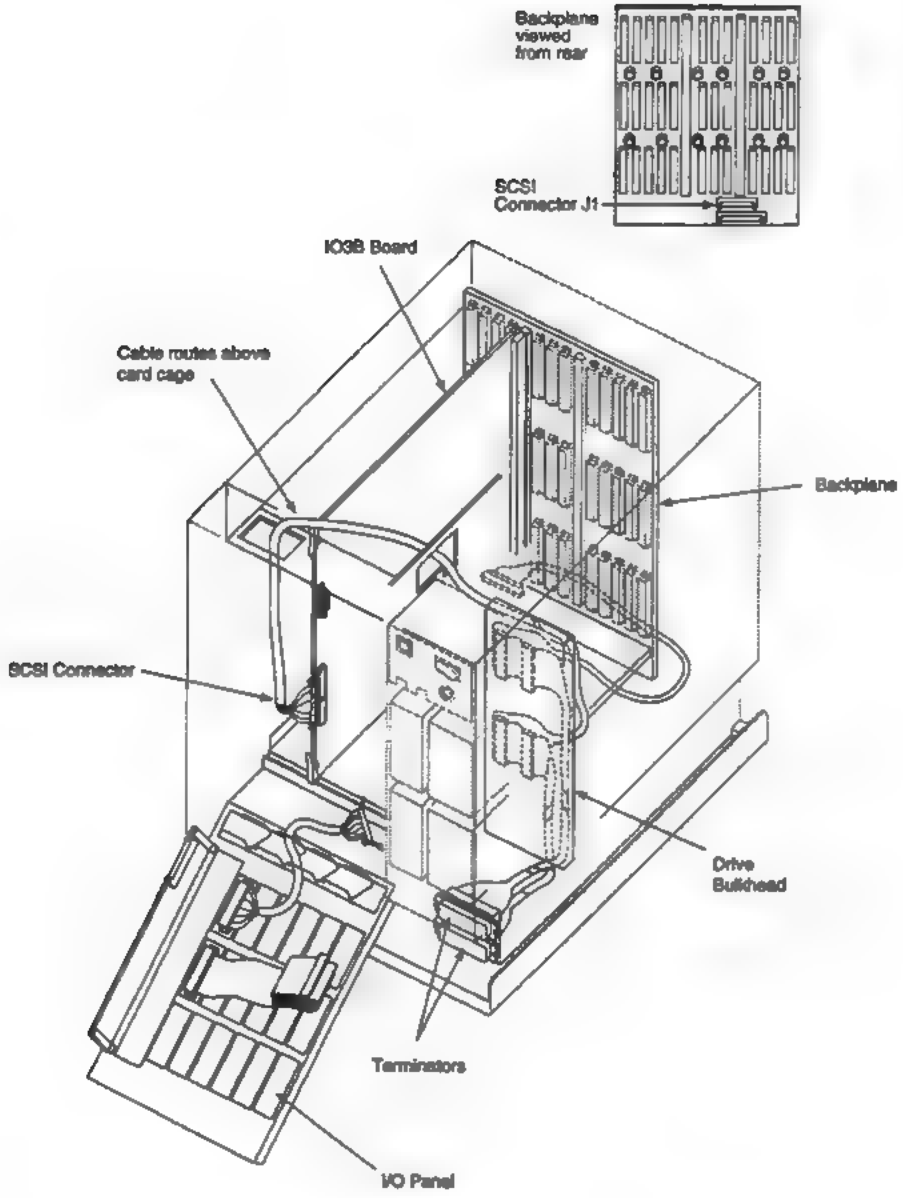


Figure 5-15 Standard System Internal SCSI Cabling

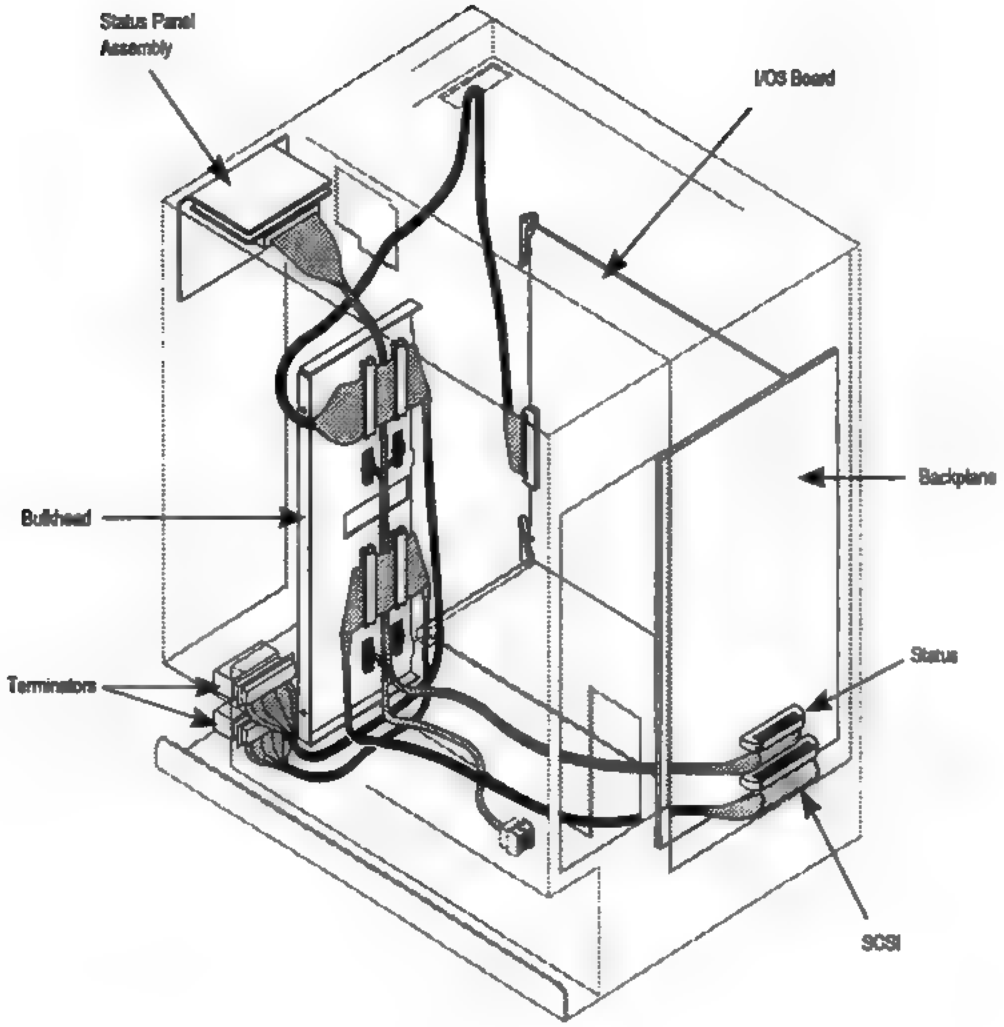


Figure 5-16 Striping the Internal Drives

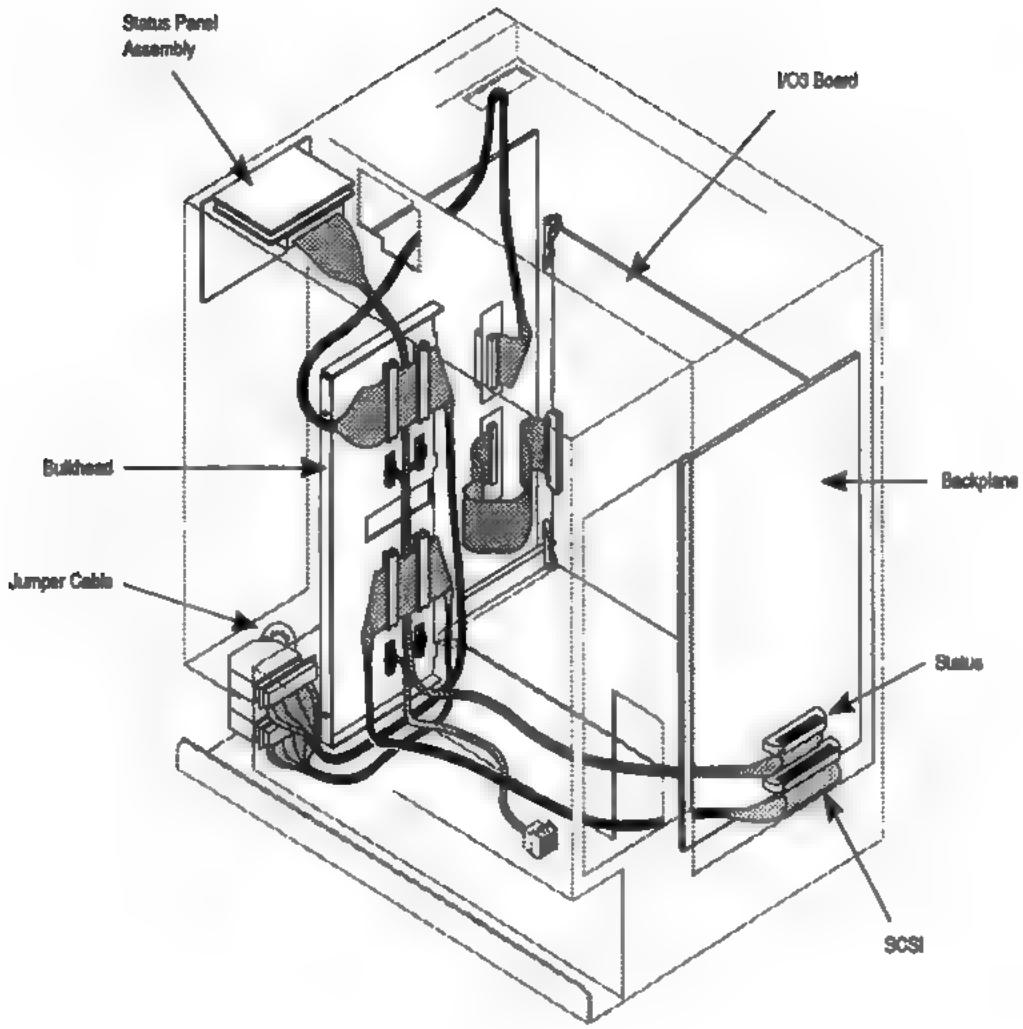


Figure 5-17 Connecting Port 1 to External SCSI Devices

Connecting Port 1 to External SCSI Devices

Port 1 requires a special flat-ribbon cable connector to the I/O panel. See Figure 5-17 for the proper cabling setup. This cable should already be in place. Do not use the other internal cable to attach port 1 to the I/O door. This connection will not work.

5.2.4 Installing the System Labels

Initial system shipments will all have a *Crimson/Server* tophat label and a W6-4DCRIMS marketing code label on the rear panel. Change the labels to reflect the configuration of the system as required. See also Chapter 2, "Configurations and Components," for information on the different marketing codes.

Note: A system configuration with 64 MB of main memory (marketing code W6-4DCR64, with one of the following suffixes: S, RE, VGX, VGXT, EG, BLG, XS, and XS24) has a rear panel label but *no* special tophat label. See also Chapter 2, "Configurations and Components," for information on the different marketing codes.

Changing the Tophat Label

Use the following procedure to change the tophat label.

1. Gently pry up the front retaining lip of the tophat with a flat-bladed screwdriver. See Figure 5-18.
2. Lift the front edge of the tophat until it clears the top panel.
3. Slide the tophat toward the rear of the chassis.
4. Remove the tophat label from the underside of the tophat by using a small pointed object, such as a nail or large paper clip.
5. Peel the adhesive strip of the new tophat label and stick it into place on the tophat.
6. Replace the tophat panel.

Changing the Rear Panel Label

You may also need to change the marketing code label on the rear panel of the system. Place the new marketing code in the location shown in Figure 5-19.

5.3 Adding Peripheral Devices

Refer to the *Peripherals Reference Guide and Man Pages* (P/N 007-1460-*xxx*), the *IRIS Crimson Owner's Guide* (P/N 007-1560-*xxx*), or the *POWER Store Rack Installation Instructions* (108-7024-*xxx*) for information on installing peripherals into a single-tower style chassis.

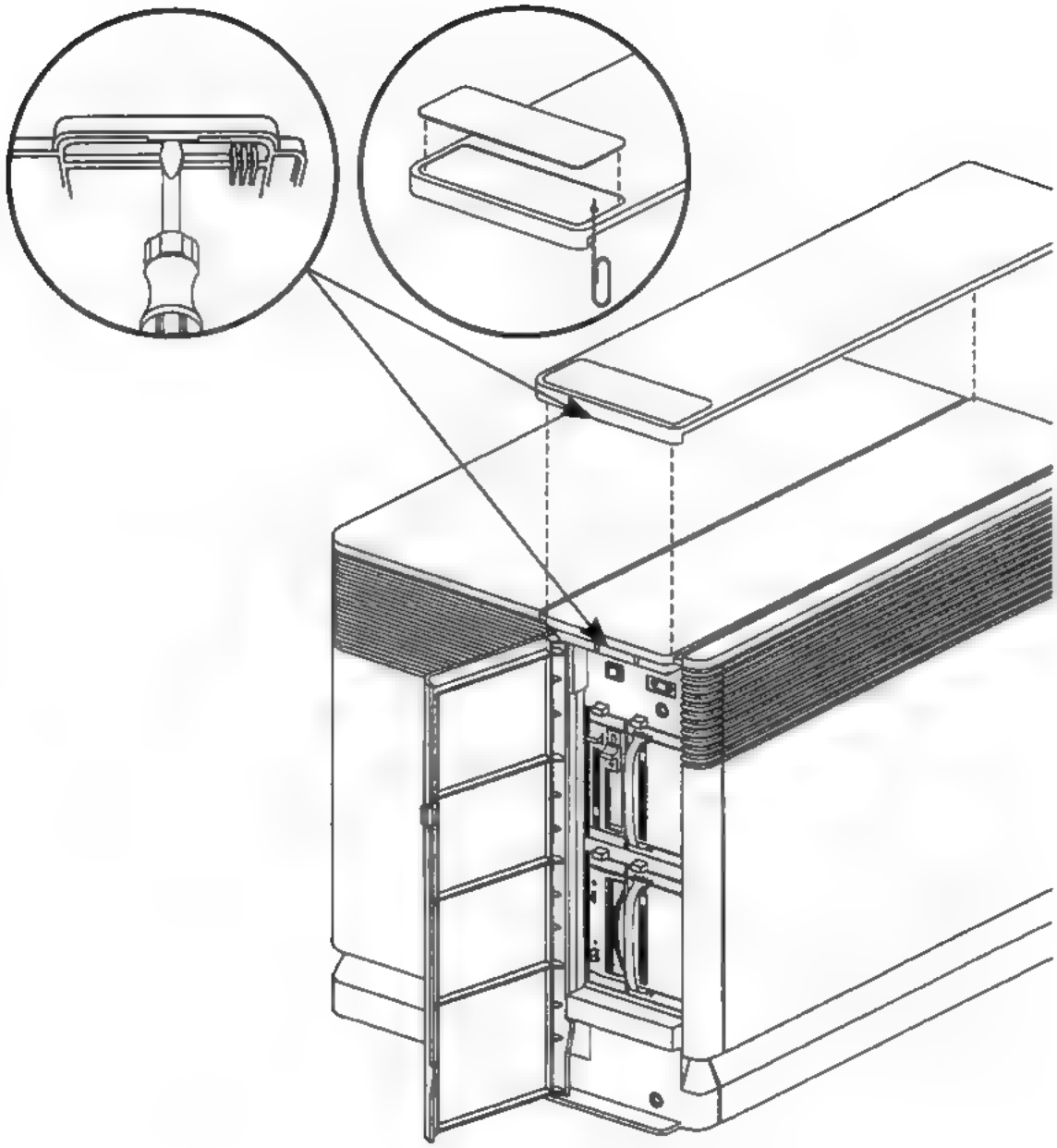


Figure 5-18 Tophat Label Placement

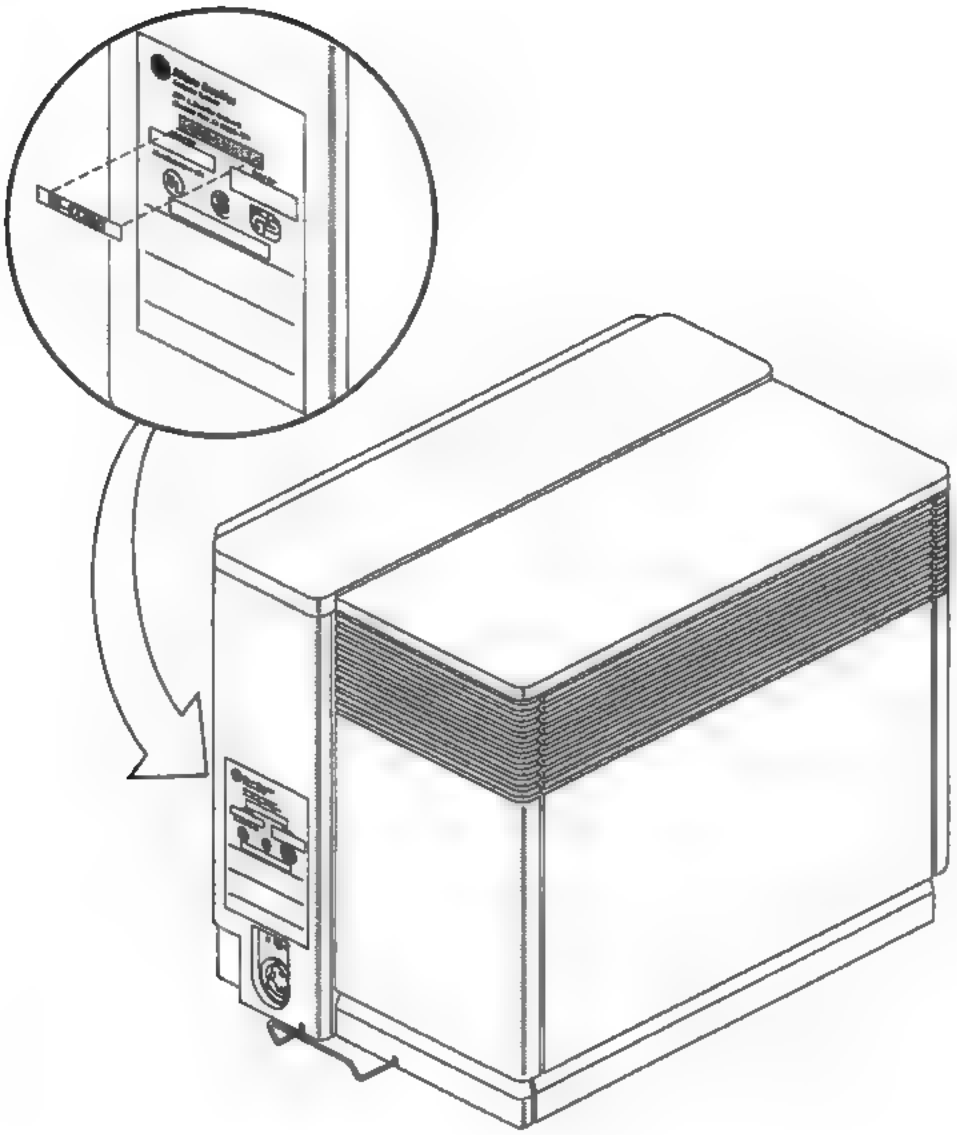


Figure 5-19 Rear Panel Label Placement

5.4 Installing Option Boards

See Chapter 4, "Chassis Tour," for board location information.

Caution: When installing a new board, check for cables to the immediate left of the affected slot. To prevent possible cable damage, hold any cables flat against their respective boards while inserting the new board.

The components are extremely sensitive to ESD. Use proper antistatic procedures while handling all components.

Note: The Crimson backplane allows you to install a VME option board without opening the rear of the chassis. To install a VME board, use slot 1 first, then add boards to the right *without skipping* any slots. This sequence is required. The backplane loops the signals from slot 5 to slots 1 through 4, and any open slot interrupts the signal flow to subsequent slots.

Skipping a slot is occasionally required to fit oversized VME boards or to improve air flow. You can skip a slot if jumper blocks are placed on the jumper pins located through the rear of the chassis and immediately to the left of the slot's P1 connector.

5.5 Setting Up the Monitor and Keyboard

The IRIS Crimson graphics configurations use three types of cable connectors, depending on the monitor type and graphics. See Figures 5-20 through 5-22.

- The 16-inch monitor uses a 13W3 to 13W3 cable connector.
- The 19-inch monitor uses a 13W3 to BNC or a 13W3 to 13W3 cable connector.
- The Crimson VGX/VGXT uses a BNC to BNC cable connector.
- The Crimson RealityEngine uses a 13W3 to BNC connector

Connect one end of the cable to the I/O panel and the other end to the monitor. Connect the keyboard to the keyboard connector on the I/O panel.

5.6 Setting Up an ASCII Terminal

The Crimson/Server configuration does not support a graphics monitor. Plug the terminal into port 1A on the I/O panel. Set the terminal to the following parameters:

- 9600 baud, full duplex
- XON/XOFF handshaking
- 8 bits
- 1 stop bit

Attach the keyboard to the keyboard connector on the terminal.

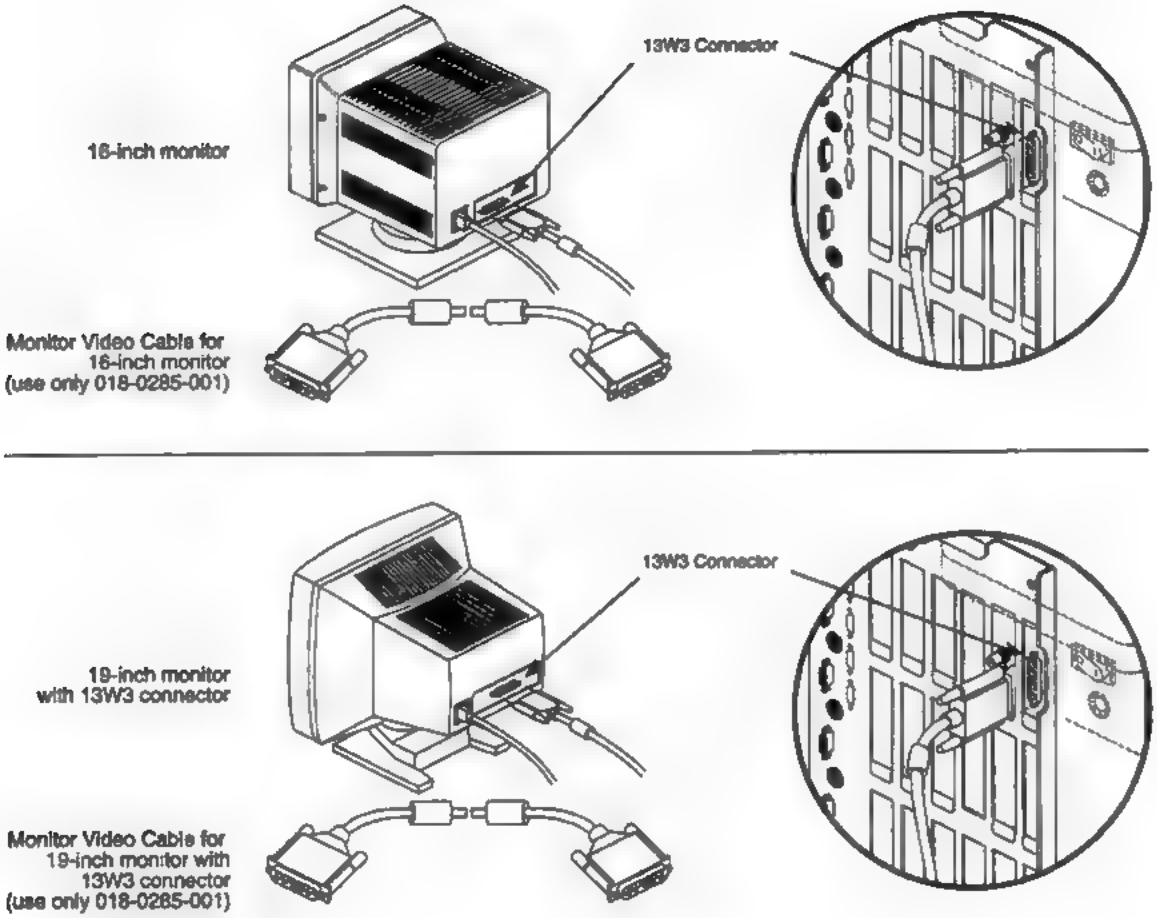


Figure 5-20 Setting Up the Monitor (Part 1)

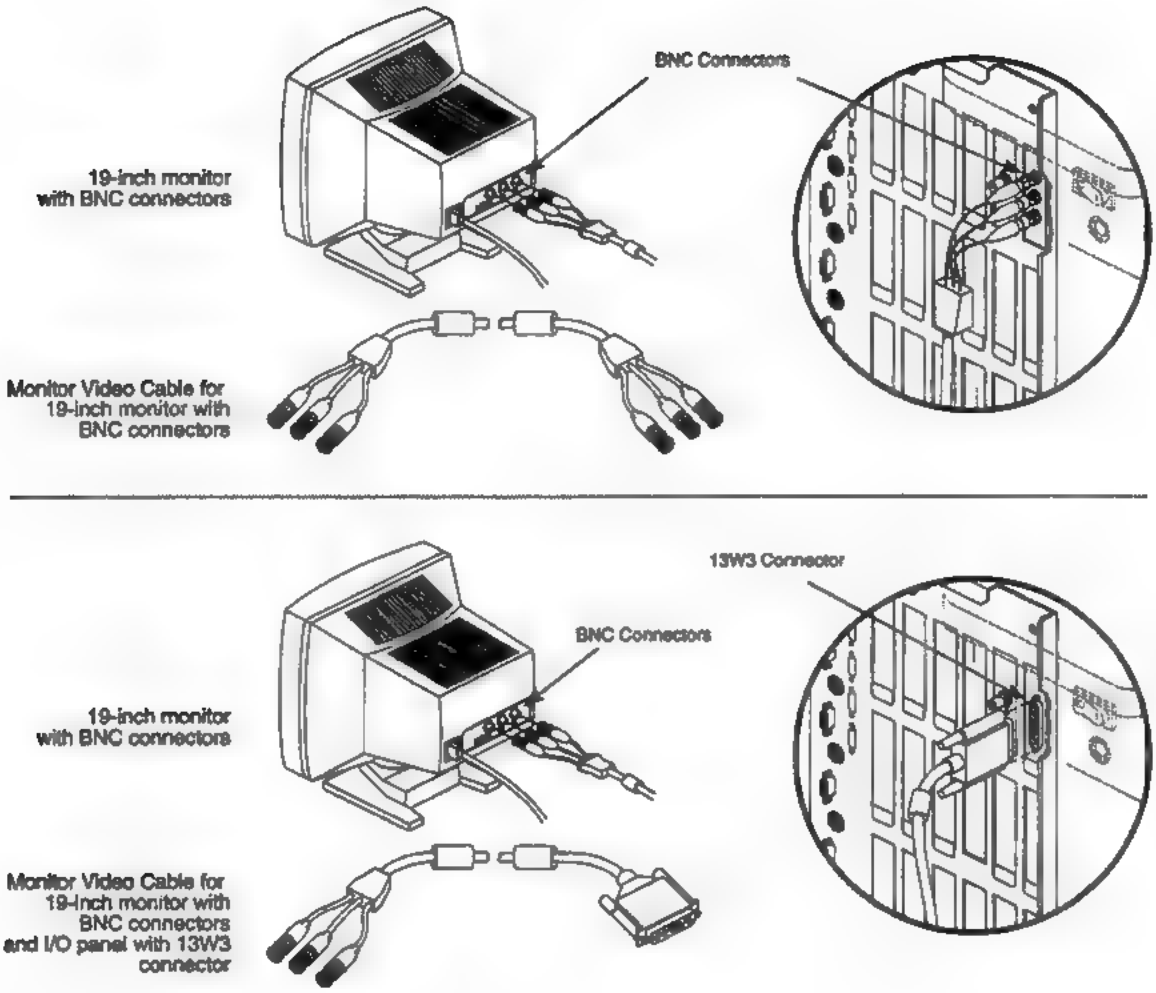


Figure 5-21 Setting Up the Monitor (Part 2)

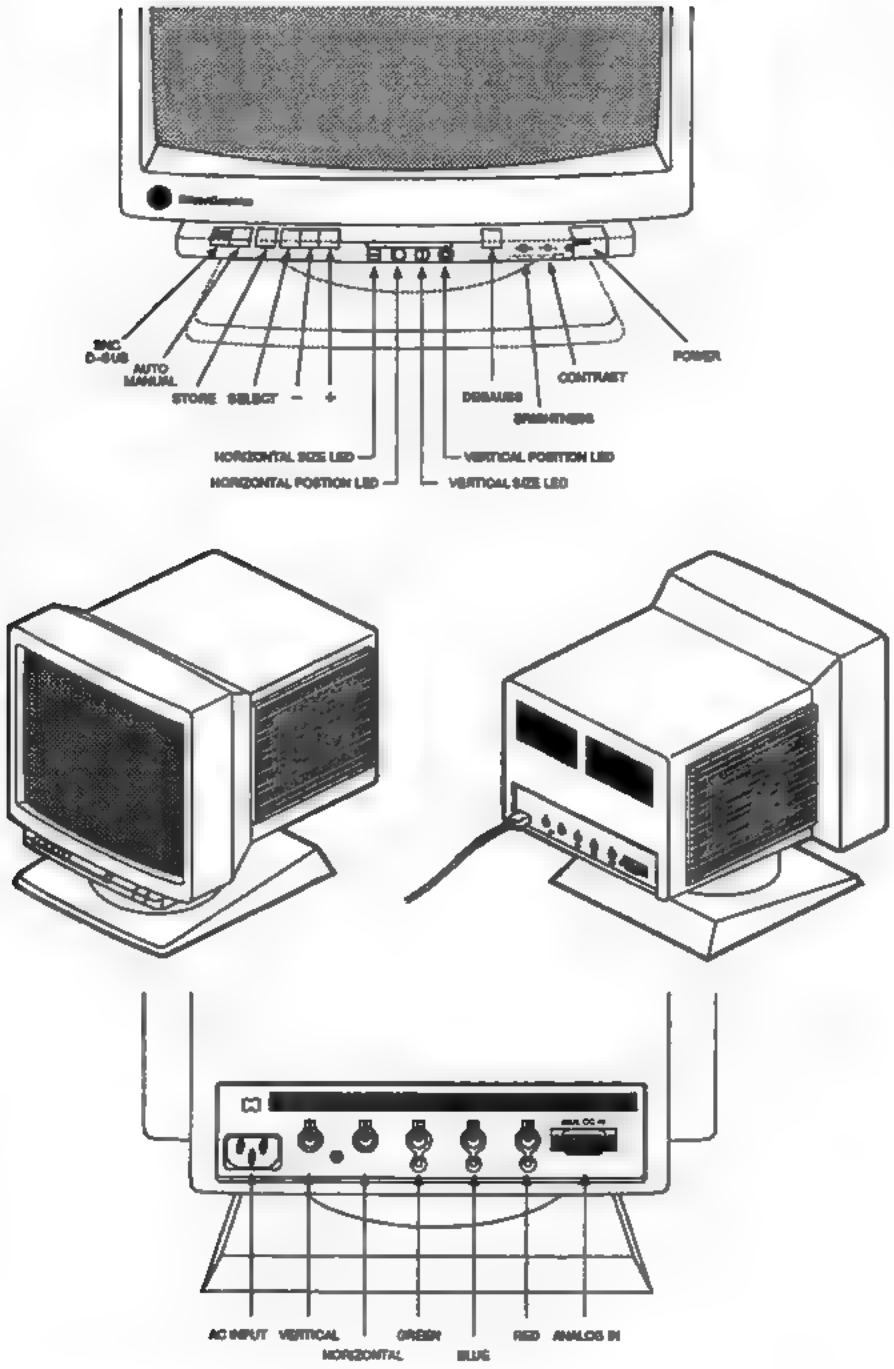


Figure 5-22 Setting Up a 21-inch Monitor

5.7 Installing Software

Before you install software on the system, it is recommended that you verify the hardware operation. Read Chapter 6, "Verifying Installation," for testing and diagnostics information. For software installation information, see your software documentation.

Note: The Crimson system requires IRIX™ release 4D1-4.0.3 or later. The RealityEngine graphics requires IRIX release 4D1-4.0.5 D or later.

Chapter 6

Verifying Installation

This chapter discusses how to verify the installation of the IRIS Crimson system.

6.1 General Procedures

Use the following procedures to bring up the system and to load diagnostics.

6.1.1 Bringing Up the System

After you install the system hardware, follow these steps:

1. Connect the main power cord to the system.
2. Connect an ASCII terminal to port 1A on the Crimson I/O panel. Ensure that the terminal is set with the following parameters:
   - 9600 baud, full duplex
   - XON/XOFF handshaking
   - 8 bits
   - 1 stop bit

   Note: It is strongly recommended that you use an ASCII terminal to run diagnostics.
3. Turn on the system, and bring up the System Maintenance Menu.

   Caution: *Important!* Systems containing the IP17 processor and RealityEngine graphics can take up to 60 seconds before the screen displays any text or graphics on powerup. Do not depress the reset button. This will only delay system boot and display.
4. Select option 5 to enter the command monitor.
5. Type **hinv** at the prompt and check the system configuration information.

   Note: Some hardware options (such as a network board) may not be recognized by the PROM monitor. These options will not be listed by the *hinv* command in this situation.

However, after you load and boot the operating system, the *hinv* command (executed at the IRIX shell) should list *most* of the system hardware options. Also note that the kernel may not recognize many video products.

Note: After you install the operating system, you can also type the following command at the IRIX prompt for details on the graphics subsystem, if present.

```
/usr/gfx/gfxinfo
```

You should get a message similar to the following:

```
Graphics board 0 is "GR2MP" graphics.
 Managed (":0.0") 1280x1024
 1 GE, 24 bitplanes, 4 auxplanes, 4 cidplanes, no Z-buffer
 GR2 revision 2, VB1.1
 HQ2 rev A, GE7 rev B, RE3 rev D, VC1 rev B,
 19" monitor
```

Note: "GR2" refers to the XS, XS24, or Elan configuration. "LG1" refers to the Entry system.

6. When you verify the basic system configuration, go to Section 6.1.2, "Installing Diagnostics."

6.1.2 Installing Diagnostics

The Crimson system provides an easier method to load standalone diagnostics. You can now install these diagnostics directly from the following:

- 1/4-inch tape
- CD-ROM

Note: The diagnostic programs are automatically stored on the hard disk after initial installation. You can invoke the diagnostics from the hard disk, thereafter.

Diagnostics Tests

The Crimson system has these categories of diagnostic tests:

- IP17 standalone tests
- Entry, XS, XS24, Elan, MG1 board and system-level tests
- VGX/VGXT graphics and system-level tests

The Crimson diagnostic tests are an extension of the integrated diagnostics environment (IDE) test suite. After installation, the system loads the IP17 tests in the */stand* directory. IRIX loads the Entry, Elan, and PowerVision tests into the */usr/diags* directory.

Loading IP17 Standalone Diagnostics

Follow these instructions to install diagnostics from the 1/4-inch tape or CD-ROM:

1. Power on the system and bring up the System Maintenance Menu.
2. Select option 3, `Run Diagnostics`. You should receive the following display:

```
Running diagnostics ...
Type "y" to select, anything else to skip to next selection.
```

Note: If system detects a CD-ROM or tape drive, it will display the next message:

```
Boot diags from CD-ROM? or
Boot diags from 1/4" tape? or
Boot diags from hard disk?
```

3. Insert the diagnostic tape or CD ROM; then select the appropriate peripheral.

Note: If you run diagnostics again, reset the system. If you do not, the system will hang.

4. After you select the peripheral, you should receive the following display:

```
Loading diagnostics ... (Press <ESC> to return to the menu)

.
.
.
Note:  Disk Write Mode is OFF (some tests which write to disk
       partition 1 are not going to run)

       If you what to run these tests, please use "f k 1" to
       turn Disk Write Mode on, and use "f w 0" to turn off the
       Warning Message Mode off.
DIAGS:
```

5. Diagnostics are now on the hard disk. If you are testing the IP17 board, go to Section 6.2, "IP17 Diagnostic Tests."

Loading Graphics and System-level Diagnostics

Use the following procedures to load graphics diagnostics (Entry, XS, XS24, Elan, or PowerVision) from CD-ROM or 1/4-mch tape. A separate CD-ROM or 1/4-inch tape contains the diagnostics files. Use the *inst* program to load the graphics diagnostics.

Note: You must install the operating system before you can run the graphics diagnostics. Refer to your operating system documentation for information on loading the software.

1. After you install the operating system software, bring up the System Maintenance Menu and select option 2, `Install System Software`.
2. Install the diagnostics files from CD-ROM or 1/4-inch tape.

3. After you complete installation, return to the System Maintenance Menu and select option 1, `Start System`. Go to Section 6.3, "Crimson Entry, XS, XS24, Elan, and MG1 Tests," or to Section 6.4, "Testing the VGX/VGXT Board Set," to invoke the diagnostics.

6.2 IP17 Diagnostic Tests

The following section describes the standalone IP17 diagnostic tests.

6.2.1 Diagnostic Commands

The following sections briefly describe the commands that you will need to use the diagnostics program.

Help Command

The diagnostics have a number of options and commands available. To see the list of command and options, enter **`help`**, **`h`** or **`?`** at the `DIAGS` prompt:

```
DIAGS: ?
```

The following information will be displayed:

```
COMMANDS:
    help:                       COMMAND(s)]
    auto execute:               a [TEST NAME]
    hardware configuration      c
    dump:                       d [s] [v]
    system configuration:       f [p#][m RANGE][d DEVS][b#][r#][v#][s#][a#]
    help:                       h 'COMMAND(s)]
    init logfile:               i
    print logfile:              l [LINES]
    menu:                       m [MENU(s)]
    quit:                       q
    execute                     x{expression[arg(s)][;expression ...]}*
count
                            where:
                            expression    testname[sequence][*count]
                            sequence      number |
(testnumbers[*loop][,...])
                            testnumbers   number | number1-number2
```

Control Characters

Invoke the following commands by pressing the **`<Ctrl>`** key along with the key noted:

- **`<CTRL-H>`** or **`DEL`** Erase single characters
- **`<CTRL-U>`** Delete entire line
- **`<CTRL-C>`** Suspend test

Note: Command lines take either uppercase or lowercase letters.

Menu Command

The menu command `m` displays the tests that can be executed. When invoked with no argument, the menu command displays the test categories. For example, when you type `m` at the Diags menu:

```
DIAGS: m
```

The following test categories are displayed:

```
CPU TEST
BUS TEST
MEM TEST
PATH TEST
IO TEST
FPU TEST
```

6.2.2 Running the IP17 Diagnostics

To perform a fast and efficient verification of the IP17 board without going through every possible diagnostics test, you can run the CPU tests and MEMORY test 1 and 9.

6.2.3 Running the CPU Tests

There are 18 CPU tests. Type `m cpu <enter>` to see the menus of all CPU tests. The screen will display the following information:

```
ptr->id cpu
mpt->desc test 8254 programming interval timer by polling, mpy->num 1
CPU1: test 8254 programming interval timer by polling
CPU2: test 8254 programming interval timer by interrupt
CPU3: test TLB as a small memory array
CPU4: test if all the TLB slots respond to probes upon address match
CPU5: test for correct virtual to physical translation via a mapped TLB entry
CPU6: map each TLB entry as invalid to cause an exception when accused
CPU7: map page non-writable, then access ampped address to cause an exception
CPU8: test matching and non-matching pid field in mapped TLB entries
CPU9: test the global bit of the mapped TLB entry
CPU10: test the uncached bit of the mapped TLB entry
CPU11: test cached vs uncached mapped TLB access
CPU12: test duarts
CPU13: instgruction cache test
CPU14: CP0 Counter & Compare register test
CPU15: primary cache parity test
CPU16: secondary cache ECC test
CPU17: RMP bus error interrupt test
CPU18: unmapped cached/uncached access test

DIAGS:
```

To run an individual CPU test, type `x cpu`*n*, where *n* is 1 through 18. Type `x cpu` to run all of the tests.

6.2.4 Running the Memory Tests

After all of the CPU tests have been successfully run, you should then run memory tests 1 and 9. To see the memory tests that are available, type **x mem**. The following information will be displayed:

```
ptr->id mem
mpt->desc memory sockets connection test, mpy->mi, 1
mem1: memory sockets connection test
mem2: address walking test
mem3: read/write patterns
mem4: address in address memory test
mem5: walking I/O memory test
mem6: memory with ecc test
mem7: mem8 [-bhw] [-v pat] RANGE - use specified address & pattern
mem8: io3 LED test
mem9: cache write-through memory test

DIAGS:
```

To run memory test 1, type **x mem1**.

Note: Do not leave a space between mem and the number of the test, or the entire suite of memory tests will execute.

The following information will display as you run memory test 1:

```
running mem 1 - memory sockets connection test

(CONNECT)

mem test pass, pass count = 1, skip count = 0

DIAGS
```

To run memory test 9, type **x mem9**. The following information will display as you execute the test:

```
running mem 9 - cache write-through memory test

(CACHEMEM)

Cached Address Test
Write 0x80ff0000'x to 0x80ff0000
Verify address 0x80ff0000
Write 0x7f00ffff'x to 0x80ff0000
Verify address 0x80ff0000
mem test pass, pass count = 1, skip count = 0

DIAGS
```

To quit the diagnostics program, enter **q** or **quit** at the prompt:

```
DIAGS: q
```

6.3 Crimson Entry, XS, XS24, Elan, and MG1 Tests

These diagnostics verify the integrity of the MG1 and graphics hardware by executing the following classes of tests:

- MG1 board diagnostics
- Entry, XS, XS24, and Elan graphics diagnostics
- screen compare checksum tests
- system level tests

6.3.1 Invoking the Diagnostics

After installing the diagnostics (see Section 6.1.2, "Installing Diagnostics"), follow these procedures to invoke the tests:

1. After the system reboot, bring up the System Maintenance Menu, and select option 1, `Start System`.
2. At the login prompt, type **`diag`**. The system displays the following:

   ```
   TERM = (vt100)
   ```

3. Press **<return>** and the system displays the following:

   ```
   Crimson Graphics:
   Automatically run Crimson [Entry, XS, XS24, Elan] diag?(y or n)
   ```

   Note: The kernel should know what type of graphics the system has.

4. Type **`y`** to display the following menu:

   ```
   CRIMSON [ENTRY, XS, XS24, ELAN] SYSTEMS DIAGNOSTICS
   ------------------------------------------------------------

   1- Quick System check
   2- Full System check
   3- Quick Server check
   4- Full Server check
   5- Quick Graphics check
   6- Full Graphics check
   7- MG1 Board Diagnostics
   8- Entry, XS, XS24, Elan Board Diagnostics
   9- System Screen Compares
   10- System Options Check
   11- View Results of diagnostics tests
   12- Automatically run selected Graphics Demos
   13- EXIT Crimson Entry (or) Elan Systems Diagnostics

   Please choose an item (1-11) >
   ```

6.3.2 Test Descriptions

Table 6-1 gives a brief description of the Entry and Elan tests.

Test	Description	Screen Compare Result
1. Quick System Check	Runs kernel, stress tests, floating point processor tests, I/O, memory, and screen compares. No IDE tests are run.	1. Jet plane 2. Jet plane with red borders 3. Wine glass 4. Silicon Graphics logo
2. Full System Check	Runs all of the above tests and all the IDE tests.	Same as above.
3. Quick Server Check	Runs a subset of the IP17 board tests, including kernel stress test, I/O, memory and system-level tests.	None
4. Full Server Check	Runs extended IP17 tests.	None
5. Quick Graphics Check	Runs the IDE graphics tests.	1. Jet plane 2. Jet plane with red borders 3. Wine glass 4. Silicon Graphics logo
6. Full Graphics Check	Runs the IDE graphics tests using multiple passes.	1. Jet plane 2. Jet plane with red borders 3. Wine glass 4. Silicon Graphics logo
7. MG1	Tests the MG1 hardware.	None
8. Entry, XS, XS24, Elan Diagnostics	Tests the hardware on the graphics board.	None
9. System Screen Compares	Performs a pixel-by-pixel comparison of images.	1. Jet plane 2. Jet plane with red borders 3. Wine glass 4. Silicon Graphics logo
10. System Options Check	Exercises system peripherals such as the tape drive, printer, and other devices.	None
11. View Results	Allows you to see the test results of all tests.	None
12. Automatically run selected Graphics Demos	Displays a series of graphic images in window screens.	No screen compare test is performed.

Table 6-1 Entry and Elan Diagnostic Test Descriptions

6.3.3 Running Diagnostics

Run option 2, `Full System Check`, to verify proper operation of the hardware after installation. If you encounter any error messages, recheck the installation, then take the appropriate action to replace the failed hardware. It is recommended that you test for one loop or pass only.

Note: Options 1, 2, 3, and 4 will request the name of a remote host for an Ethernet test. To bypass this test, simply press **<return>**.

Log File Results

The diagnostics program creates a log file in the *usr/tmp* directory that contains results for each test. An example of a log file is */usr/tmp/quickgr.log*. This particular file corresponds to the "Quick System Check" test. To view the results of the log file, type the following at the IRIX prompt:

more *<log file name>*

Note: To return to the main menu, type **main.ide** or **menu**. See Table 6-2 for other important commands.

Action	Command
Quit testing	<cntrl> c
Pause screen display	<cntrl> s
Continue screen display	<cntrl> q
Suspend current process	<cntrl> z
Restart diags in foreground	fg test#
Check diagnostic log	check */usr/tmp/fullsys.log0*

Table 6-2 Diagnostics Commands

Screen Compare Tests

The screen compares verify the functionality of the graphics by displaying an image and comparing the values generated by each image against the checksums expected for that image. The diagnostics use *gold* file checksums to check if the graphics subsystem displays the proper screen image.

The graphics monitor displays the images while the ASCII terminal shows a running log of the test in progress. As you are running the tests, you should see a display similar to the following on the ASCII terminal:

```
    .
    .
    .
INFO:  400: CP microcode RAM data test
INFO:  410: CP ucode addr test
INFO:  410: CP microcode RAM address test
INFO:  420: CP ucode full test
INFO:  420: CP microcode RAM full test
    .
    .
    .
```

MG1 Tests

Option 7 tests the integrity of the MG1 hardware by executing the following types of tests:

address test uses a walking one bit to generate and test unique addresses

data test checks for shorts on the data bus through a walking one bit test and a pattern test

pattern test determines proper operation of the memory modules

Data can be written out to the GIO bus through the command mapper (for three-way transfers), directly to the FIFOs, or through the special bypass registers. See Section 1.5.4, "MGI (GRINCH) Board," and Figure 1-7 for more information on the MG1 architecture.

You will receive the following display when you select option 7:

```
MG1 Tests
1. All MG1 Tests
2. Mg1Reset
3. Mg1 Control Reg Test
4. Command Mapper Test
5. EEprom Test
6. PIO Test
7. Fifo Tests
8. 3 Way Test
9. Stress Test
10. GIO Test"
11. Exit from Menu
```

Run option 10, `Full System Test`, for a complete checkout of the MG1 hardware. Run the individual tests to isolate problems as required.

Table 6-3 provides a description of the MG1 diagnostic tests.

Test	Description
1. Full System Test	Executes all of the tests below.
2. MG1 Reset	Resets the MG1 and graphics boards and checks if the boards return in stable condition. This test also determines if the board returns the correct ID.
3. MG1 Cont. Reg Test	Checks the two control registers using a write-read-compare program with different data patterns.
4. Command Mapper	Tests the address and data lines by writing then reading for expected values at address 0 of the command mapper. The test checks for any *stuck* bits. The test also writes alternating patterns to each location in the command mapper, then reads and verifies the data.
5. EEpromTest	Reads and verifies the current contents of the flash EEPROM. This test does not destroy the contents of the EEPROM.
6. PIO Test	Transmits programmed I/O through the bypass register, then reads the bypass register.
7. Fifo Tests	Checks the address and data FIFO by writing values, by checking the read registers for the expected values. This test also fills the FIFOs with unique values to check for high and low water mark filling and emptying capability.
8. 3 Way Test	Initializes the command mapper, writes GIO addresses to the FIFOs, then checks the FIFO for the correct address.
9. Stress Test	Places the board in different operational modes and checks if the board returns in stable condition.
10. GIO Test	Writes a value to the GIO address register, then reads register 1. The test checks that the eight high-order bits contain the same value as the GIO address register.

Table 6-3 MG1 Test Descriptions

Running Graphics Tests Manually

The */usr/diags/scripts* has a directory that you can use in place of the menu-driven selections. These diagnostics test specific areas of the graphics hardware such as the geometry engines.

Below is a list of screen compare commands:

ccompge tests the geometry engine (GE) circuitry.

ccompppep checks the pp/ep (poly processing and edge processing).

ccompras tests the raster system.

ccompspin spins and rotates objects.

ccomploop executes a specified number of test loops for either the previous screen compare test or a new screen compare test. See the following note for more information.

Note: The *ccomploop* command uses the following format:

ccomploop [cn] [count]

[c] indicates *continue* with the previous test command.

With this option, the previous pass/fail counts in the log file will not be cleared.

[n] indicates *new* test. The user must then specify a screen compare command, such as *ccompge*.

With this option, the previous pass/fail counts in the log file will not be cleared.

[count] determines the number of test loops.

These screen compare tests will provide either a PASS or FAIL result followed by possible error location information. The test also provides a test result of each of the spans, where appropriate.

Graphics Test Completion

This completes the testing of the Entry and Elan board set. Check the *usr/tmp/fullsys.log0* for any failures.

6.4 Testing the VGX/VGXT Board Set

This section describes how to test the PowerVision graphics board set, VGX and VGXT.

6.4.1 Test Menus

The diagnostics provide two types of menus:

- a set of board diagnostics
- a set of screen compare images

Board Diagnostics

These tests check the GM3, GE6, RM2, and DG1 circuitry functionality by writing data patterns into SRAMs, DRAM, VLSI devices, and control registers. The tests then read back the data and compare it with expected values. These microcode tests also check data paths, control logic, and signal lines for correct operation. These tests produce test messages that point to suspect circuitry and/or boards.

Note: Some tests interact with more than one board at a time. Consider this carefully during troubleshooting.

Screen Compare Tests

The VGX/VGXT compare scripts use CRC codes to verify that the VGX/VGXT board set is sending out images instead of huge gold files. The images that appear on the graphics terminal will be the last images placed in the frame buffer before the testing begins, so you will see random images flickering on the graphics terminal until the screen displays appear. Check Table 6-4 for a list of screen displays that should appear.

The screen compares verify the functionality of the VGX/VGXT board set by displaying an image (for example X-29, wireframe jet, or PowerVision soda can) and by comparing the values generated by the each image against the CRC codes expected for that image. The diagnostics use CRC codes to check whether or not the image has been properly displayed; you don't have to verify the image visually.

Note: The diagnostics load the microcode (if any is required) from the */usr/diags/usr/gfx/ucode* file.

Test	Time	Description	Screen Compare Results
Quick Graphics Check	18 minutes	Runs a subset of the full IDE tests. Tests all the boards in the VGX.	Smooth silver X-29 on blue-gray background, wireframe jet, and PowerVision soda can.
Entire Graphics Test	30 minutes	Runs all the IDE tests, followed by screen compare.	Smooth silver X-29 on blue-gray background, wireframe jet, and PowerVision soda can.
GM3 Test	6 minutes	Runs the IDE tests on the 68020 host interface, the triangle engine, and pixel bus interface. If you run this diagnostic with the -q option, the full DRAM tests and 3-way combination tests are skipped.	None
GE6 Test	6 minutes	Runs the IDE tests to check the GE, PE, CD, VR, and TE interface.	None
RM2 Test	20 minutes	Runs the RM2 IDE tests.	None
DG1 Test	2 minutes	Runs the DG1 IDE tests.	None
Screen Compares	2 minutes	Checks generated images against expected CRC codes.	Smooth silver X-29 on blue-gray background, wireframe jet, and PowerVision soda can.

Table 6-4 PowerVision Diagnostic Tests

6.4.2 Invoking PowerVision Diagnostics

Follow these procedures to invoke the diagnostics:

1. After the system reboot, bring up the System Maintenance Menu, and select option 1, `Start System`.
2. At the login prompt, type **`diag`**. The system displays the following:

```
TERM = (vt100)
```

3. Press **<return>** and the system displays the following:

```
VGX/VGXT Graphics:10-span Alpha system
Automatically run Power Vision diagnostics (y or n)?
```

4. Type **`Y`** to display the following menu:

```
PowerVision Graphics Diagnostics
------------------------------------------------
(Time estimates apply to 10 span system)
1- Quick Graphics Subsystem Check1
2- Test Entire Graphics Subsystem
3- GM3 Board Diagnostics
4- GE6 Board Diagnostics
5- RM2 Board Diagnostics
6- DG1 Board Diagnostics
7- CRC System Screen Compares
8- EXIT PowerVision Diagnostics
Please choose an item (1-8) >
```

Note: The `Entire Graphics Subsystem` test option has the same GM3, GE6, RM2, and DG1 tests (automatically run in sequence) as the individual board tests.

6.4.3 Running the Board Tests

Follow these steps to test the PowerVision board set.

1. After you log in as `diag` and receive the PowerVision diagnostics prompt, type **`y`**. The master PowerVision diagnostic menu appears, and the VGX board set configuration is listed at the top of the menu.
2. First verify the basic functionality of the PowerVision board set with option 2, `Quick Graphics Subsystem Check`. This diagnostic verifies the basic functionality of the PowerVision board set. If you receive error messages, use the appropriate individual board test to isolate failures. Before you begin testing, you should check the *ide.log* in */usr/tmp/ide.log0* for any prior failure entries.

   Note: There are two *ide.log* files, 0 and 1. Crimson uses *ide.log0*. Currently, only the dual-headed SkyWriter™ system uses both *ide.log0* and *ide.log1*.

To return to the main menu, type **`main.ide`** or **`menu`**. See Table 6-5 for other important commands.

Action	Command
Quit testing	<cntrl> c
Pause screen display	<cntrl> s
Continue screen display	<cntrl> q
Suspend current process	<cntrl> z
Restart diags in foreground	fg test#
Check diagnostic log	check */usr/tmp/fullsys.log0*

Table 6-5 Diagnostics Commands

3. Type `1` during the `Quick Graphics Subsystem Check`, and diagnostic information similar to the following appears:

```
ide>> INFO:  10: GE/PE Stress Tests
INFO:Background GE Stress Started
INFO:Background PE Stress Started
INFO:GE Stress Pattern
INFO:PE Stress Pattern
INFO:GE & PE Stress Pattern
INFO:Background GE Stress Stopped
INFO:Background PE Stress Stopped
INFO:GE Stress Clash
INFO:GE Background PASS    30267  FAIL        0
INFO:GE Pattern A       PASS     6000    FAIL        0
INFO:PE Pattern C       PASS     6000    FAIL        0
```

4. If all the diagnostics run successfully, the IDE prompt appears and a "passed" message is displayed.

```
Diagnostic Success (<CR> to continue)
```

   If any failures occur, they are logged into */usr/tmp/ide.log*.

5. If all the tests pass, the VGX/VGXT board set is operating correctly. However, if you receive failure messages, note the test name description, message, and run the full set of IDE tests. Choose option 2. A display similar to the following appears:

```
Begin GM3 diagnostics
Welcome to unix ide
ide>> INFO:  10: GM PIO Revision ID Test
INFO:          revision level 0
INFO:  11: GM PIO Reset Test
INFO:  12: GM PIO Unreset Test
INFO:  13: GM PIO Initial Cond Test
INFO:  20: GM SRAM Walking 1 Test
INFO:  21: GM SRAM Address Test
INFO:  22: GM SRAM Pattern Test
INFO:  30: GM DRAM Walking 1 Test
INFO:  31: GM DRAM Address Test
INFO:  32: GM DRAM Pattern Test
INFO:  33: GM DRAM Cycle Type Test
INFO:  40: GM PIO DFIFO Control Test
INFO:  41: GM PIO FIFO Control Test
INFO:  42: GM PIO FIFO Walking 1 Test
INFO:  43: GM PIO FIFO Pattern Test
INFO:  50: GM 3WAY FIFO Control Test
             repeating with word swapped
INFO:  51: GM 3WAY FIFO Walking 1 Test
             repeating with word swapped
INFO:  52: GM 3WAY FIFO Pattern Test
             repeating with word swapped
INFO:  53: GM 3WAY FIFO Combo Test
INFO:  60: GM AASRAM Walking 1 Test
INFO:  61: GM AASRAM Address Test
INFO:  62: GM AASRAM Pattern Test
       70: GM AASRAM Walking 1 Test
       71: GM AASRAM Address Test
       72: GM AASRAM Pattern Test
       85: GM DMA swapper test
ide>> pix
INFO:  10: PIX TO Bus Test
INFO:  11: PIX TADDR Test
INFO:  12: PIX BANK Test
INFO:  13: PIX C and Z Bus Test
INFO:  14: PIX Copy Test
INFO:  15: PIX Pattern Control Test
INFO:  16: PIX Stipple Control Test
INFO:  17: PIX Ydone Test
INFO:  18: PIX Xdone Test
INFO:  19: PIX BUFdone Test
INFO:  20: PIX Bye Swizzle Test
Done
Begin GE6 diagnostics
Welcome to unix ide
ide>> INFO:Resetting GE6 board
INFO:  100: GE6 board reset
INFO:  100: GE6 board reset test
INFO:  GE6 board revision 1
INFO:  200: OPSTATE test
INFO:  200: OPSTATE test
INFO:  300: CP map data test
INFO:  300: CP command map RAM data test
INFO:  310: CP map addr test
INFO:  310: CP command map RAM address test
INFO:  320: CP map full test
INFO:  320: CP command map RAM full test
INFO:  400: CP ucode data test
INFO:  400: CP microcode RAM data test
INFO:  410: CP ucode addr test
INFO:  410: CP microcode RAM address test
INFO:  420: CP ucode full test
INFO:  420: CP microcode RAM full test
INFO:  500: GE ssr test
INFO:  500: GE SSR test
INFO:  510: GE ucode data test
INFO:  510: GE microcode RAM data test
INFO:  520: GE ucode addr test
```

6. If all the diagnostic tests are successful, the screen displays the IDE prompt appears and a "passed" message:

```
Diagnostic Success (<CR> to continue)
```

7. The diagnostic detects an error condition if the tests do not finish, or if you see an "interrupted" or "stopped" message. If an error occurs, answer **a** to discontinue testing. Return to the main diagnostic menu and write down the error message shown in the *ide.logfile*. Then select an individual board test from the test menu to verify the failure.

8. For example, the following screens display error messages from a failing RM2 board:

```
INFO:     16: IMP Alphaless Confirmation Test
INFO:      17: IMP Memory Test
INFO: Test pass 1 out of 1
INFO: Writing Bank 0
INFO: Writing Bank 1
INFO: Writing Bank 2
INFO: Writing Bank 3
INFO: Reading Bank 0
ERROR: (17) IMP Memory Test (bits 0-31): X:0x0000 Y:0x0000 BANK:0
(BD0 SP0 IMP0) exp:0xffffffff got:0x006545ff
<Stopped>
ide>>
Errors detected in the ide logfile
ERROR: (17) IMP Memory Test (bits 0-31): X0x0000 Y:0000 BANK:0
(BD0 SP0 IMP0) exp:0x
```

6.4.4 Running the Screen Compare Tests

1. After the microcode tests have run successfully, run the screen compare tests from the main PowerVision menu.

   Note: The Quick or Entire Graphics Subsystem Check displays the screen compares at the end of the tests. You do not need to select the screen compares individually from the menu.

2. If applicable, type **7** to select the screen compares from the menu. As the following displays appear on the ASCII terminal, the graphics monitor will display an X-29, a wireframe jet, a rotating cylinder, and the PowerVision soda can.

```
PowerVision system CRC tests...
loaducode: finished loading gm3.u
loaducode: finished loading cp.u
loaducode: finished loading ge.u
loaducode: finished loading vr.u
loaducode: finished loading pe.u
loaducode: finished loading te.u
loaducode: finished loading aatab.b
gl_init_pipe() only
loaducode: finished loading amRAM.u
5 span system
Comparing files ...
sys.1 PASSED
sys.2 PASSED
num lines: 824
max size: 50
num points: 11534
bounds (-0.975618 -0.089218 -0.574548) to (0.716532 0.274094
0.574548)
sys.3 PASSED
```

3. This completes the testing of the PowerVision board set. Check the */usr/tmp/ide.log* for any failures.

6.5 RealityEngine Graphics Tests

These diagnostics verify the integrity of the RealityEngine system graphics hardware by executing the following classes of tests:

- GE8, RM4(T), and DG2 board diagnostics
- screen compare checksum tests
- system level tests

6.5.1 Invoking the Diagnostics

After installing the diagnostics (see Section 6.1.2, "Installing Diagnostics"), follow these procedures to invoke the tests:

1. After the system reboot, bring up the System Maintenance Menu, and select option 1, `Start System`.
2. At the login prompt, type **`diag`**. The system displays the following:

   ```
   TERM = (vt100)
   ```

3. Press **<return>** and the system displays the following:

   ```
   RealityEngine Graphics:
   Automatically run Reality Engine diagnostics?(y or n)
   ```

4. Type **`Y`** to display the following menu:

```
REALITY ENGINE SYSTEMS DIAGNOSTICS TEST TIME (hr:min)
-----------------------------------------------------

(Average test time based on a 16MB 4D420RE system with 10 spans)

 1- Pipe Select
 2- Quick System check ..................... 1:34
 3- Full System check ...................... 2:11/loop
 4- Quick Server check ..................... 2:11
 5- Full Server check ...................... 0:40/loop
 6- Quick Graphics check ................... 1:05
 7- Full Graphics check .................... 1:13
 8- GE8 Board Diagnostics .................. Menu
 9- RM4 Board Diagnostics .................. Menu
10- DG2 Board Diagnostics .................. Menu
11- CRC System Screen Compares ............. 0:43
12- System Options Check .................... Menu
13- View Results of diagnostic tests ........ Menu
14- Automatically run selected Graphics Demos
15- EXIT RealityEngine Systems Diagnostics

Pease choose an item (1-15)>
```

6.5.2 Running Diagnostics

It is recommended that you run option 3, `Full System Check`, of the system-level menu to verify proper operation of the hardware after installation. If you encounter any error messages, recheck the installation, then take the appropriate action to replace the failed hardware. Run the test for one loop or pass only after initial installation.

Note: Options 2 through 5 will request the name of a remote host for an Ethernet test. To bypass this test, press **<return>**.

Board-level Tests

Run the individual board diagnostics when you suspect a problem with a particular board. You can invoke these tests by selecting item 8, 9, or 10 on the system menu. Sections 6.5.4 through 6.5.6 describe these diagnostics.

These tests check the GE8, RM4(T), and DG2 circuitry functionality by writing data patterns into SRAMs, ASICs, VLSI devices, and control registers. The tests then read back the data and compare it with expected values. These microcode tests also check data paths, control logic, and signal lines for correct operation. These tests produce test messages that point to suspect circuitry and/or boards.

Note: Some tests interact with more than one board at a time. Consider this carefully during troubleshooting.

If you receive error messages, use the appropriate individual board test to isolate failures. Before you begin testing, you should check the *ide.log* in */usr/tmp/ide.log0* for any prior failure entries.

Note: There are two *ide.log* files, 0 and 1. Crimson uses *ide.log0*. Currently, only the dual-headed SkyWriter system uses both *ide.log0* and *ide.log1*.

To return to the main menu, type **exit**. See Table 6-2 for other important commands.

Screen Compare Tests

The screen compares verify the functionality of the graphics by displaying an image and comparing the values generated by each image against the checksums expected for that image. The diagnostics use *gold* file checksums to check if the graphics subsystem displays the proper screen image.

The RealityEngine compare scripts use CRC codes to verify that the RealityEngine board set is sending out images instead of huge gold files. The images that appear on the graphics terminal will be the last images placed in the frame buffer before the testing begins, so you will see random images flickering on the graphics terminal until the screen displays appear. See Section 6.5.3, "System-level Graphics Tests," for a list of screen displays that should appear.

The screen compares verify the functionality of the RealityEngine board set by displaying an image (for example a jet plane or wine glass) and by comparing the values generated by each image against the CRC codes expected for that image. The diagnostics use CRC codes to check whether or not the image has been properly displayed; you don't have to verify the image visually.

Note: The diagnostics load the microcode (if any is required) from the */usr/diags/usr/gfx/ucode* file.

ASCII Terminal Output

The graphics monitor displays the images while the ASCII terminal shows a running log of the test in progress. As you are running the tests, you should see a display similar to the following on the ASCII terminal:

```
    .
    .
    .
Welcome to unix ide
ide>> ide>> ide>> INFO: Starting supertest PIO_regs ...
INFO: PIO_regs: starting subtest Soft Reset (10) ..... PASSED
INFO: PIO_regs: starting subtest Verify Write Read (11) ..... PASSED
INFO: PIO_regs: starting subtest Walk Video0 Interrupt (12) .....
PASSED
    .
    .
```

Log File Results

The diagnostics program creates a log file in the *usr/tmp* directory that contains results for each test. An example of a log file is */usr/tmp/quickgr.log*. This particular file corresponds to the "Quick System Check" test. To view the results of the log file, type the following at the IRIX prompt:

more *<log file name>ide.log*

Note: To return to the main menu, type `menu.RE`. See Table 6-6 for other important commands.

Action	Command
Quit testing	<cntrl> c
Pause screen display	<cntrl> s
Continue screen display	<cntrl> q
Suspend current process	<cntrl> z
Restart diags in foreground	fg test#
Check diagnostic log	check */usr/tmp/fullsys.log0*

Table 6-6 Diagnostics Commands

6.5.3 System-level Graphics Tests

Table 6-7 gives a brief description of the system-level graphics tests.

Test	Description	Screen Compare Result
1. Pipe Select	For SkyWriter only. Selects either pipe 0 (right side) or 1 (the left-side).	
2. Quick System Check	Runs kernel, stress tests, floating point processor tests, I/O, memory, and screen compares. No IDE tests are run.	1. Jet plane 2. Jet plane with red borders 3. Wine glass 4. Silicon Graphics logo
3. Full System Check	Runs all of the above tests and all the IDE tests.	Same as above.
4. Quick Server Check	Runs a subset of the CPU board tests, including kernel stress test, I/O, memory and system-level	None
5. Full Server Check	Runs extended CPU tests.	None
6. Quick Graphics Check	Runs the IDE graphics tests.	1. Jet plane 2. Jet plane with red borders 3. Wine glass 4. Silicon Graphics logo
7. Full Graphics Check	Runs the IDE graphics tests using multiple passes.	1. Jet plane 2. Jet plane with red borders 3. Wine glass 4. Silicon Graphics logo
8. GE8 Board Diagnostics	Tests the GE8 hardware.	None
9. RM4 Board Diagnostics	Tests the RM4(T) hardware.	None
10. DG2 Board Diagnostics	Tests the DG2 hardware.	
11. CRC System Screen Compares	Performs a pixel-by-pixel comparison of images.	1. Jet plane 2. Jet plane with red borders 3. Wine glass 4. Silicon Graphics logo
12. System Options Check	Exercises system peripherals such as the tape drive, printer, and other devices.	None
13. View Results of diagnostic tests	Allows you to see the test results of all tests.	None
14. Automatically run selected Graphics Demos	Displays a series of graphic images in window screens.	No screen compare test is performed.

Table 6-7 RealityEngine System Test Descriptions

6.5.4 GE8 Tests

This section describes the geometry engine (GE8) diagnostics test. You will see the following display when you select option 8 on the system menu:

```
RealityEngine Graphics Diagnostics for GE8 - Test Time (min:sec)
----------------------------------------------------------------
(Average test times based on a 4D420RE system w. 16MB of memory)

1 - Quick Check of GE8 ................................ 0:41
2 - Full Check of GE8 ................................. 8:56
3 - GE8 - MPG1/PIO Registers Test ..................... 0:23
4 - GE8 - CP2/GEs JTAG Connectivity Test .............. 0:06
5 - GE8 - GEs Connectivity Test ....................... 0:05
6 - GE8 - PIO/CP2 Data Transfer Test ................... 0:25
7 - GE8 - CP2/GEF Connectivity & CP2 Scan Test ......... 0:44
8 - GE8 - 3-Way Basic Data Transfer .................... 0:10
9 - GE8 - ODMA/Host Data Transfer Test ................. 0:19
10- GE8 - IDMA/CP2 Data Transfer Test .................. 0:09
11- GE8 - GEF Functional Test ......................... 4:51
12- GE8 - I860 Functional Test ........................ 0:07
13- GE8 - CP2 Functional Test ......................... 0:06
14- GE8 - MPG1 Functional Test ........................ 0:03
15- GE8 - GE8 Interrupt Test .......................... 0:05
16- GE8 - MP Bus Stress Test .......................... 0:03
17- GE8 - VC Bus Test ................................. 0:26
18- EXIT from menu

Please choose an item (1-18) >
```

Run option 2, `Full Check of the GE8`, for a complete checkout of the GE8 hardware. Run the individual tests to isolate problems as required.

Table 6-8 provides a description of the GE8 diagnostic tests.

Test	Description
1. Quick Check of GE8	Executes a subset of the available GE8 tests by running these types of tests: a PIO register test, a JTAG control test, a GE connect test, a PIO FIFO scan test, a CP ucode scan, a PB scan, a GEF scan, and a three-way transfer test. Each of these tests is described in this table.
2. Full Check of GE8	Executes all of the GE8 tests.
3. MPG1/PIO Registers Test	Writes and reads the MPG1 registers, walks 1s and 0s through return in stable condition. This test also determines if the board returns the correct ID.
4. CP2/GEs JTAG Connectivity Test	Verifies the connectivity between the CP (command processor) and the geometry engines (GEs) using the JTAG test.
5. GEs Connectivity Test	Verifies the connectivity between all the GE8s using the JTAG protocol. These checks include a chain test, an ID code check for each GE, a stuck-bit check, a short check, and clock tests.
6. PIO/CP2 Data Transfer Test	Tests the data transfer between the programmable I/O (PIO) registers and the CP2 (command processor) through various subtests. These include the following tests: • the PIO FIFO registers write, read, and reset tests. • the PB PIO connectivity test that checks the packet buffer (PB) in the GEF ASIC to the PIO by downloading a ping test, an output DMA (ODMA) register test, and a reset test. • the PB DRAM PIO test that checks the GEF DRAMs. • the PIO tests that verifies the full connectivity path the checking the links from the host to CP2 to GEF to MPG1 and back to the host.

Table 6-8 GE8 Diagnostic Test Descriptions

Test	Description
7. CP2/GEF Connectivity and CP2 Scan Test	Executes a number of subtests including the following: • CP2 to GEF JTAG test • PIO FIFO scan checks the 33-bit MPG1 output data bus to the CP2 using JTAG tests. • CP2 UCODE scan verifies the command processor microcode in SRAM (shadow RAM) using JTAG tests. • PB scan downloads a packet buffer (PB) to the GEF diagnostic registers and executes JTAG tests. • GEF scan executes a JTAG test to verify a functional handshake to the GEF ASIC.
8. 3-Way Basic Data Transfer	Consists of three tests: an offset, command 0, and Pipe 1 tests. The offset test checks four different offset values. The command 0 and pipe 1 tests are *sanity* checks that verify the MPG1 3-way functionality.
9. ODMA/Host Data Transfer Test	Performs several functional tasks such as walking 1s and 0s across the 32-bit bus, testing different settings and offsets of word counts and data.
10. IDMA/CP2 Data Transfer Test	Downloads CP and GE microcodes and then starts the IDMA transfer. The test passes the results through the MPG ODMA word count register.
11. GEF Functional Test	Consists of seven subtests, including a bus give test, a hold bus test, a cache test and a walk test. In each of these tests, a 32-bit word is sent to the output direct memory access (ODMA) word count register and then read by the host through the PIO register.
12. I860 Functional Test	Checks the functionality of the Intel i860XP
13. CP2 Functional Test	Performs about 22 command processor (CP) subtests including an 8, 12, 16, 32, and 64-bit conversion test, a branch test, a register test, and a shadow RAM (SRAM) test.
14. MPG1 Functional Test	Verifies the functions of the MPG (multiprocessor bus to graphics) ASIC. Verifications include packing data, converting data, and checking the interaction between the GEFs (geometry engine FIFOs) and the CP (command processor).

Table 6-8 (continued) GE8 Diagnostic Test Descriptions

Test	Description
15. GE8 Interrupt Test	Tests various GE interrupts such as GEF interrupt, FIFO overrun, and ODMA interrupt. The test sends the interrupts to all the CPUs and then performs walking 1's and 0's across the interrupt status register.
16. MP Bus Stress Test	Checks the MP bus interface and data transfer by loading data into memory then transferring it to the GE through the PIO, 3-way, and input DMA randomly. The test verifies the data received on the host.
17. VC Bus Test	Tests the interface between the GE8 and DG2 by initializing the DG2 across the VC bus and then executing function manager tests. Note: For a description of the function manager tests, see Section 6.5.6, "DG2 Tests."
18. Exit from Menu	

Table 6-8 (continued) GE8 Diagnostic Test Descriptions

6.5.5 RM4 Tests

This section describes the raster memory (RM4/T) board tests. You should see a display similar to the following when you select option 9 on the system menu:

```
Results will be logged in: /usr/tmp/rm4.log0
Venice Graphics Diagnostics for RM4 Test Time(min:sec)
-------------------------------------------------------------------
(Average test times based on a 420RE system w. 16MB of memory)

1- Quick Check of RM4 ..................................... 07:00
2- Full Check of RM4 ...................................... 13:30
3- RM4 - Connectivity Test ................................ 00:15
4- RM4 - TBus/RBus/Vbus Connectivity Test ................. 02:00
5- RM4 - TBus Signature Test .............................. 02:40
6- RM4 - IMP (framebuffer) Memory Test .................... 00:40
7- RM4 - TA/TD (texture) Memory Test ....................... 00:40
8- RM4 - Configuration Verification Test ................... 00:10
9- RM4 - Reset the RM4 ..................................... 00:10
10- EXIT from menu

Please choose an item (1-10) >
```

Table 6-9 provides a description of the RM4 tests.

Test	Description
1. Quick Check of RM4	Executes all the RM4 tests once.
2. Full Check of RM4	Executes all the RM4 tests twice.
3. Connectivity Test	Tests the chip-to-chip connectivity of the RM4(T) board by executing a number of tests, including the following: *id code test* - verifies the chip id code for each chip. *stuck-at test* - drives a logic 0 and 1 on the output of each driver and verifies that it is present at each input pin *short test* - runs a sect of vectors to test for shorts. *status test* - ensures that all ASCI ready lines are driven to idle when the board is reset.
4.TBus/RBusVbus Connectivity Test	Checks the TBus and RBus connectivity between the RM4 and GE8 boards by walking a 1 and 0 down the 48 bits of the data bus and 7 bits of the address bus for each GEF on the GE8. The test also checks the read back bus connectivity between the IMP buffers (IBs) on each RM4 and the CP2 on the GE8 board.
5. TBus Signature Test	Consists of a series of files that test the CRC signatures of the RM4 ASICs. The signature tests diagnose faulty ASICs.

Table 6-9 RM4 Test Descriptions

Test	Description
6. IMP (frame buffer) Test	Tests the frame buffer memory by walking a 1 and a 0 across the data and address lines of each IMP and generating a memory pattern in each 16-bit location.
7. TA/TD (texture) Memory Test	Tests the texture address (TA) and texture data (TD) address by walking a 1 and 0 across these buses. The test also writes a pattern to texture memory then verifies the pattern.
8. Configuration Verification Test	Checks for the presence of a DG2 board and reports the number RM4 boards available in the system.
9. Reset the RM4	Resets the RM4 board(s) and checks if the boards return in stable condition. This test also determines if the board returns the correct ID.
10. Exit From Menu	

Table 6-9 (continued) Raster Memory Test Descriptions

6.5.6 DG2 Tests

This section describes the display generator (DG2) diagnostic tests. When you select option 10 on the system menu, you should receive a display similar to the following:

```
*Results will be logged in: /usr/tmp/dg2.log0
Venice Graphics Diagnostics for DG2 Test Time(min:sec)
-------------------------------------------------------------------
(Average test times based on a 420 system w. 16MB of memory)

1- Quick Check of DG2 ..................................... 2:00
2- Full Check of DG2 ...................................... 2:30
3- Memory Tests............................................ 0:30
4- Register Tests ......................................... 0:15
5- Function Manager Sram Tests ............................ 0:15
6- Xmap Memory Tests ...................................... 0:30
7- JTag Connectivity Tests ................................ 0:30
8- HV List Tests............................................ 0:30
9- XMAP CRC Tests........................................... 0:30
10- Cursor Tests............................................ 0:30
11- EXIT from menu

Please choose an item (1-11) >
```

Table 6-10 describes the DG2 diagnostics.

Test	Description
1. Quick Check of DG2	Executes a subset of the DG2 tests including the following: • system connectivity • XMAP CRC • memory • HV list • cursor memory
2. Full Check of DG2	Tests the following areas: • system connectivity • XMAP CRC • memory • registers • DG2 connectivity • HV list • cursor memory
3. Memory Tests	Executes all of the DG2 diagnostics memory tests.
4. Register Tests	Checks the control registers using a write-read-compare program with different data patterns.
5. Function Manager SRAM Tests	Tests the shadow RAM (SRAM) of the function manager by loading test display data into the function manager, then checking the contents of the SRAM after execution.
6. Xmap Memory Test	Tests the Xmap color lookup tables (CLUTs), Xmap display ID tables, and the Xmap control SRAM.
7. JTag Connectivity Test	Performs a component-to-component connectivity test to check for shorts and disconnections.
8. HV List Tests	Checks the HLIST and HLIST functionality by verifying the horizontal (H) and vertical (V) list call process. This test checks if the test calls are present at various memory locations and devices, and if the FIFO flag full activates after a certain amount of calls or events.
9. XMAP CRC Test	Performs a cycle redundancy check on the XMAP ASICs by executing a JTAG and boundary scan tests.
10. Cursor Tests	Tests the cursor glyph controller using various cursor types.
11. Exit from Menu	

Table 6-10 DG2 Test Descriptions

6.5.7 Running Graphics Tests Manually

The */usr/diags/scripts* has a directory that you can use in place of the menu-driven selections. These diagnostics test specific areas of the graphics hardware such as the geometry engines.

Below is a list of screen compare commands:

ccompge tests the geometry engine (GE) circuitry

ccompppep checks the pp/ep (poly processing and edge processing)

ccompras tests the raster system

ccompspin spins and rotates objects

ccomploop executes a specified number of test loops for either the previous screen compare test or a new screen compare test. See the following note for more information.

Note: The *ccomploop* command uses the following format:

ccomploop [cn] [count]

[c] indicates *continue* with the previous test command.

With this option, the previous pass/fail counts in the log file will not be cleared.

[n] indicates *new* test. The user must then specify a screen compare command, such as *ccompge*.

With this option, the previous pass/fail counts in the log file will not be cleared.

[count] determines the number of test loops.

These screen compare tests will provide either a PASS or FAIL result followed by possible error location information. The test also provides a test result of each of the spans, where appropriate.

This completes the testing of the RealityEngine board set. Check the */usr/tmp/fullsys.log*0 for any failures.